NSW PH MT HVDC Functional Requirements

DB.3 Background Report

Step-by-step guide on functional requirements and parameter ranges definition for HVDC building blocks

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Shaping power transmission

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4044	Generic functional requirements and parameter ranges for HVDC building blocks based on existing literature and references

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1. Executive summary

The North Sea Wind Power Hub (NSWPH) consortium is responsible for planning and pre-developing a series of hub-and-spoke projects that will enable large-scale North Sea offshore wind deployment and its integration in the energy system. The hub-and-spoke are based on elementary block types that are used in association to build the distributed hub scenarios. The NSWPH methodology to develop the concept is structured in three phases: pre-feasibility (2020-2021), feasibility (2021-2022) and pre-FEED (2022-2023). This report focuses on pre-FEED phase and has the aim to assess from a transmission system operator (TSO) perspective how to derive and specify functional requirements as well as parameter ranges for radial and meshed multi-terminal HVDC systems and their associated modular HVDC building blocks based on an adequate Simplistic Test Benchmark (STB) environment. The STB consists of sub-benchmarks allowing to verify functional requirements and parameter ranges according to four functional groups: (i) DC control; (ii) DC protection; (iii) DC ancillary services and (iv) DC operational regimes.

The functional requirements and parameter ranges are iteratively improved throughout different use cases selected in the sense of expandability and future development stages of Multi Terminal HVDC systems from radial topologies, extended radial and meshed DC grid. Extensions of the use cases will increase the complexity of the MTDC grid and will challenge the proposed simplistic benchmark model. Lessons learned through this iterative process are incorporated into the simplistic test benchmark so that both the model and the test environment are improved after each proof-of-concept process iteration.

Modelling

The STB environment is built exclusively with simplistic DC grid components presented in the first part of the report. Average Value Models (AVM) of the MMC half-bridge converter have been proposed to model the behavior of converter inner and outer controls (up to a certain level of detail), behavior of the converter during DC short circuit faults as well as behavior of the converter during energization. A simplistic cable model based on pi-sections has been proposed that represents the current and voltage evolution during transient events. To consider the cable characteristics during DC fault transients a new model for travelling wave propagation is suggested avoiding the need of a complex frequency dependent cable model. The STB environment and parameter ranges definition have been validated through a proof-of-concept based on PSCAD simulations for the three proposed use cases.

DC grid control functional group

For the functional group related to DC grid control the main aspects that have been analyzed are the DC steady state voltage ranges definition, the fixed DC voltage control mode, the primary and secondary DC voltage control, and the impact of DC current limiting reactor value on the voltage stability. Using Graph theory, a STB has been proposed to estimate the steady state DC voltage whatever the DC grid size. The results obtained suggest that the steady-state voltage range specification need to be wide enough to allow future system expansion. The steady state voltage range impact the minimum “pole-to-ground” voltage for normal operation which is an important parameter to be specified for the equipment design to fulfill the operational requirement of the converter station, such as active power and reactive power transfer capability.

For fixed DC voltage control mode, two parameters have been identified which impact the DC voltage stability: the response time of DC voltage controller and DCR size. For each combination of these two factors, the proposed methodology based on STB allows to estimate the damping ratio and natural frequency of the system. Hence, it is possible to select the DCR value and response time that satisfy the damping ratio limit. For example, with a response time of PI controller of 50 ms the DCR should be less than 600 mH to respect a damping ratio limit of 10%.

For the selected DC voltage control droop scheme, the impact of droop gain, DCR value and the response time of PI controller have been analyzed for controllability and disturbance management. The results show that the steady state voltage profile is predominantly determined by the assigned droop gains where the dynamic behavior in case of disturbance is mainly determined by response time with little influence of the DCR size. An STB based on analytical formula has been proposed which allows to estimate the peak voltage in case of disturbance.

A sensitivity analysis shows that Post Fault Active Power Recovery requirements are determinant for the sizing of the control droop gain, response time and DCR value. According to the grid code required time to reach 90% of pre-contingency active power level (200 ms), some combinations of these three factors will not be acceptable. For example, in case of 300 mH for DCR with 5% of droop gain, the response time of PI controller shall be less than 40 ms to satisfy the grid code requirements.

For the Secondary DC voltage control, the objectives and the needs for this control were demonstrated through simulations using a system consisting of the developed AVM model. Relevant parameters necessary for this control were also proposed.

DC protection functional group

Functional requirements and parameters ranges for DC grid protection have been identified based on a fully-selective fault clearing strategy and AC system criteria to ensure frequency stability of AC system in term of permanent (2 GW) and temporary (3 GW) stop of active power. To identify the temporary stop duration, an STB based on a single machine equivalent model of a synchronous area has been developed. It allowed to conclude that a temporary stop duration of 4s can be acceptable for AC system with equivalent inertia as low as 1.1s considering a future European power system based on Ten Years Network Development Plan (TYNDP) trajectories. To ensure the maximum loss of infeed during a fault, the acceptable number of blocked MMCs is strictly limited. During a fault transient the MMC can block due to overcurrent and/or over- and undervoltage. To cope with the criterion of overcurrent a new functional requirement based on maximum DC current MMC blocking criteria is proposed and extensively analyzed. A DC fault ride through profile considering over- and undervoltage at the DC side of the converter has been provided. Impact of MMC sub-module energy value on the temporary undervoltage during fault is investigated and an STB is proposed to evaluate the minimum MMC energy level requirements for several undervoltage limits. STBs have been suggested to allow an extensive sensitivity analysis to determine the parameter ranges for DC reactors, DC circuit breaker operation time, current capability and energy absorption. As an example, for an operating time of 3 ms and MMC blocking criteria of 3pu (based on the nominal DC current), a DC reactor size of 280 mH DC is required at each line end. Proof-of concept of DC protection functional group through EMT simulations allows to conclude that the STB environment can effectively be used to determine functional requirement and parameter ranges for the HVDC building block components.

DC ancillary services functional group

In the functional group ancillary services different energization sequences have been investigated. Main design parameters for the cable energization are the overcurrent and undervoltage limits that need to be respected. Based on that an appropriate value for the Pre-Insertion Resistor (PIR) in-between 50-100Ω has been determined. The uncontrolled energization of a converter from a DC side can be necessary if a converter was disconnected due to maintenance. The impact on the DC grid should be limited during energization. In this context a comprehensive STB is proposed which allows to specify the design of the PIR at the converter output.

DC operating regimes functional group

A new proposal of AC/DC converter operating states is presented (starting from CENELEC report) that allows to consider the specificities of the onshore and offshore HVDC building blocks. The start-up of the grid in various configurations has been investigated using use radial grid and meshed grid. An STB has been developed to represent the main behavior during the grid start-up. It was found that the grid can start-up using various sequences controlling the DC voltage at an early or a late stage. The energization can be also performed in a sequential manner – energizing each cable/converter individually – or simultaneously. The particular case of the energization of the grid as individual point-to-points was also demonstrated. The main critical step is the deblocking of the converters charged from the DC side (typically offshore converters) that induces a large inrush current and voltage oscillations. A possible solution to avoid large inrush current is to deblock the offshore converters sequentially, one after the other.

The analyses carried out within each functional group allowed to establish several Simplistic Test Benchmark though which is was possible to refine the functional requirements and parameter ranges that have been updated in the tendering material deliverable.

2. Acronyms

ACCB: AC Circuit Breaker

AAM: Average Arm Model

AVM: Average Value Model

BFI: Breaker Failure Identification

CAPEX: Capital expenditures

CBC: Current Breaking Capability

CM: Connection Modes

DBSB: Double Bus Single Breaker busbar configuration

DBS: Dynamic Braking System

DCCB: DC Circuit Breaker

DC-PoC: DC Point-of-Coupling

DCR: DC Reactor

DMR: Dedicated Metallic Return

EIT: Electric Insertion Time

FCR: Frequency Containment Reserve

FCS: Fault clearing Strategy

FRR: Frequency Restoration Reserve

FS-FCS: Full-Selective FCS

HB-MMC: Half Bridge MMC

MMC: Modular Multilevel Converter

MMC-WF: MMC connected to the Wind Farm

MTDC: Multi-Terminal HVDC grid

OCO: Opening Closing Opening

OWF: Offshore Wind Farm

OWT: Offshore Wind Turbine

OV = Over Voltage

PoC: Point of Connection

PSCAD: Power Systems Computer Aided Design

PtP: Point to Point

PIR: Pre-Insertion Resistor

PS: Permanent Stop

STB: Simplistic Test Benchmark

TYNDP: Ten Years Network Development Plan

TS: Temporary Stop

TSO: Transmission System Operator

UV = Under Voltage

3. Introduction

The Paris Agreement defined a goal of net zero greenhouse gas emissions by 2050. Offshore wind energy is one of the main renewable energy sources to achieve this goal, as reflected in the 2050 capacity target of 300 GW set by the European Commission (EC). This large-scale offshore wind deployment and its integration in the energy system needs international coordination, long-term policy targets and a robust regulatory framework.

The North Sea Wind Power Hub (NSWPH) consortium was created in 2017 to cope with those challenges. It consists of main actors in the North Sea: Energinet, Gasunie and TenneT. The Project Scoping workstream is responsible for planning and pre-developing a series of hub-and-spoke projects, which are based on the innovation solutions proposed by NSWPH to ensure cost-effective and step-by-step deployments. A simplified schematic drawing of bilateral interconnected distributed energy hubs between Denmark, the Netherlands and Germany is shown in Figure 1.

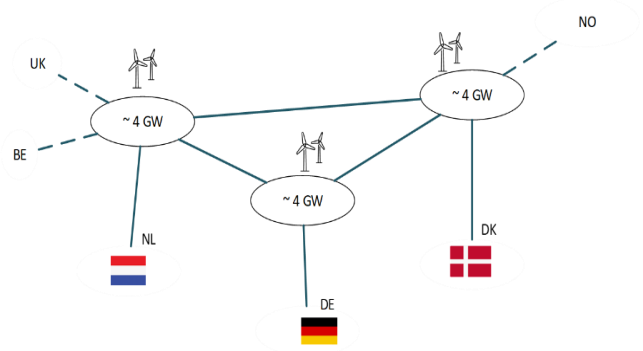


Figure 1: NSWPH / National Initiatives – Bilateral interconnected distributed-hubs

Pre-feasibility studies started in 2019 and the definition of a preferred configuration is foreseen for 2023. The project construction is expected to start in 2025 with a provisional commissioning of the first hub-and-spoke which is estimated for 2035.

The NSWPH methodology to develop the concept is structured in three phases: pre-feasibility (2020-2021), feasibility (2021-2022) and pre-FEED (2022-2023). In each step, the range of considered project configurations decreases and the level of detail in studies increases. The pre-feasibility phase had the aim to perform a screening of 10-20 alternative hub configurations. The feasibility phase focused on techno-economic assessment of the best selected configurations, considering the technical feasibility, in term of topology and protection.

The main objective of the pre-FEED phase is to assess from a transmission system operator (TSO) perspective how to derive and specify functional requirements as well as parameter ranges for radial and meshed multi-terminal HVDC systems and their associated modular HVDC building blocks. The work is intended to be carried out in the sense of preparing a specification for the FEED phase.

3.1. Objectives

ENTSO-E published grid connection codes that cover Requirement for Generators (RfG) [1], for consumption Demand Connection Code (DCC) [2] and for High Voltage Direct Current Connections [3]. For the NSWPH project, all three connection codes are relevant, due to the vision of connecting offshore generation (windfarm) and demand, while enabling power exchange between the different countries. The grid codes specify functional performance requirements at the AC point-of-connection between the system operator and the connected plant. These functional requirements include active power control, reactive power control, voltage and frequency operational ranges and fault-ride-through requirements. However, the grid codes are in principle designed for connecting generation, consumption via HVDC to the main onshore power system, (with inertia) and not to a 100 % inverter-based offshore isolated system. Thus, the purpose and technical feasibility of each specific requirement when connecting HVDC to an inverter based offshore system must be questioned.

A central issue is to investigate to which extend it is possible to apply the existing system security regulations and grid codes mentioned to the NSWPH concept. In this regard, it is important to analyze any shortfalls and gaps of the existing functional requirements that need to be addressed. An evident gap is the fact that the current version of the EU grid-codes does not include functional requirements for grid-forming control, nor functional requirements for multi-terminal HVDC operation which can turn out to be important for the NSWPH design. There may be other less evident requirements of the existing grid codes which need to be updated or refined to accommodate the system integration of energy islands.

Specifying functional requirements for innovative systems where there is no or very limited experience in operating gives rise to a dilemma. This dilemma is explained by the ENTSO-E in their offshore development position paper [4] as the vicious cycle, which must be broken through innovative demonstration projects. Figure 2 explains the complexity of TSOs and manufacturers when attempting to develop new systems. The manufacturers require functional specifications in order develop solutions, but TSOs cannot draft sufficiently detailed specifications due to limited operational experience, thus creating an endless loop: a vicious cycle.

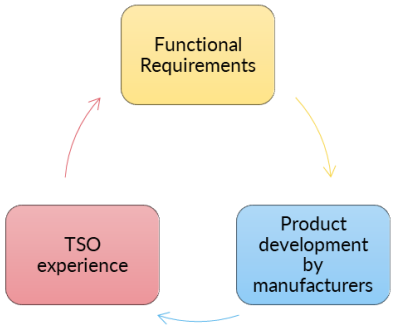


Figure 2: Vicious cycle of TSOs and manufacturers in developing new systems

The main objective of this study is to assess from a Transmission System Operator (TSO) perspective how to derive and specify functional requirements as well as parameter ranges for radial and meshed Multi Terminal HVDC (MTDC) grids and its associated modular HVDC building blocks such as AC/DC converter stations at offshore and onshore side and the DC switching station. The work is focused on the DC Point-of-Coupling (DC-PoC) of the modular HVDC building blocks and superordinated/overarching MTDC system functionalities in a radial or meshed DC grid topology. Within this study the DC protection system has been chosen to cope with the onshore limits of Frequency Containment Reserve (FCR) and Frequency Restoration Reserve (FRR). To respect that constraint, a fully selective fault clearing strategy as proposed in [5] is considered.

This report incorporates the simplistic benchmark test environment and the lessons learned into a comprehensive documentation on how to specify functional requirements and parameter ranges for MTDC grids at a common DC-PoC interface. This guide explains the step-by-step approach for the following aspects:

- → Development of simplistic benchmark model environment
- → Development of testing procedures for the HVDC building blocks
- → Definition and refinement of functional requirements and parameter ranges

The guide outlines to which extend generic test[1] procedures are applicable for the definition of functional requirements of the different building blocks. The limits of such a generic test procedure are highlighted and possible non-generic test[2] procedures are also included. The lessons learned from the iterative improvement of functional requirements and parameter ranges are incorporated and evaluated. The evaluation includes a list of pros and cons regarding the genericity of each functional requirement and the dedicated testing procedure. The guide also provides an overview of the impact of upper and lower parameter ranges change on a given functional requirements.

3.2. Methodology

The global methodology that has been followed for SoW A and SoW B is depicted in Figure 3. The overall goal of SoW B is to develop a methodology on how to refine functional requirements and parameter ranges for the modular HVDC building blocks in MTDC grids based on an adequate Simplistic Test Benchmark (STB) environment. In the NSWPH methodology, the main components of the MTDC grid system are the so-called modular HVDC building blocks, defined as follows:

- → Offshore HVDC Converters
- → Onshore HVDC Converters
- → DC Switching stations

The STB consists of sub-benchmarks allowing to verify functional requirements and parameter ranges according to their simulation time scale needs (i.e. static, dynamic, transient analysis). The STB have been defined for the following four functional groups:

- → DC control
- → DC protection
- → DC operational modes
- → DC ancillary services

Similarities among different sub-benchmarks developed for different functional group and/or building blocks are analyzed, with the intention to narrow down the different options and to ease the work necessary to define the functional requirements and parameter ranges for MTDC grids.

[1] A generic test procedure is understood as a test procedure that is applicable for a specific building block independently from the MTDC grid.
[2] A non-generic test procedure is understood as a test procedure that is either dependent on the MTDC grid structure or not representable by simplistic grid models.

The simplistic benchmark test environment is iteratively improved throughout the different use cases depicted in section 4.2. The different use cases are selected in the sense of expandability and future development stages of MT-HVDC systems from radial topologies to meshed topologies. Extensions of the use cases will increase the complexity of the MTDC grid and will challenge the proposed simplistic benchmark model. Lessons learned through this iterative process is incorporated into the simplistic test benchmark so that both the model and the test environment are improved after each proof-of-concept process iteration.

The benchmark test environment is built exclusively with simplistic DC grid components presented in 5 (i.e. controlled voltage & current sources, equivalent DC grid capacitance, inductance, resistance) excluding complex component models. The aim is to generalize and simplify the test environment as much as possible while remaining sufficiently accurate and representative of the considered phenomena according to EMT models and to propose adequate testing procedures for functional requirement validation of different building blocks. As already mentioned, it is understood that the simplistic benchmark must be robust in terms of grid expandability. Furthermore, the simplistic benchmark model of a building block should be compliant with the functional requirement to be tested. Some functional requirements involve dynamic or transient representation of the DC grid and dedicated components, whereas for others a static representation provides a convenient response.

It is understood that the overall goal is to come to a systematic and modular design of the building blocks at the DC-PoC enabling grid extensions. In other words, the dependency of the design on the surrounding grid should be as small as possible to allow modular DC grid planning (expandability) and to reduce calculation time. Therefore, each building block will be built and tested utmost independently so that generic testing procedures can be defined while simplifying the DC grid as much as possible.

Proof-of-concept

The objective of the proof-of-concept is to validate the proposed benchmark test environments for each HVDC building block based on a specific use case. Each use case is modeled in PSCAD, and necessary EMT simulation test cases are defined. For accuracy purposes, detailed models for grid components need to be considered in this part. The proof of concept is divided into four main steps:

- → Definition of test scenarios for use case simulation
- → Development of use case in PSCAD
- → Use case simulations
- → Iterative refinement of STB

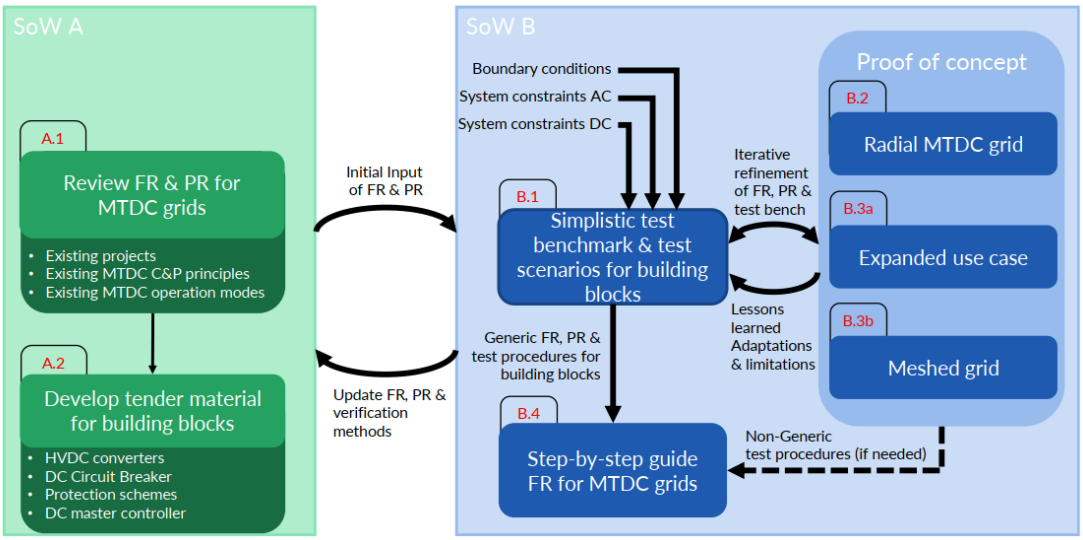


Figure 3: Workflow for global approach for SoW A and SoW B

4. Tools & input data

4.1. Tool used in the study

→ **PSCAD v4.6.3 (64bit):** PSCAD is a commercial tool for simulation and analysis of power systems. It is a time-domain software used for the Electro Magnetic Transient simulations. In accordance with the Client, it has been decided to use PSCAD v4.6.3 (x64bit) in combination with Intel Fortran Compiler IF 15. PSCAD has been used for the development of the complete use cases (see section 4.2) as well for the development of STB.

4.2. Use cases

Three use cases have been proposed by the client:

→ Use case 1.1: radial grid

→ Use case 1.2: extended radial grid

→ Use case 2: meshed grid

The diagram of use case 1.1 is provided in Figure 4 along with naming conventions.

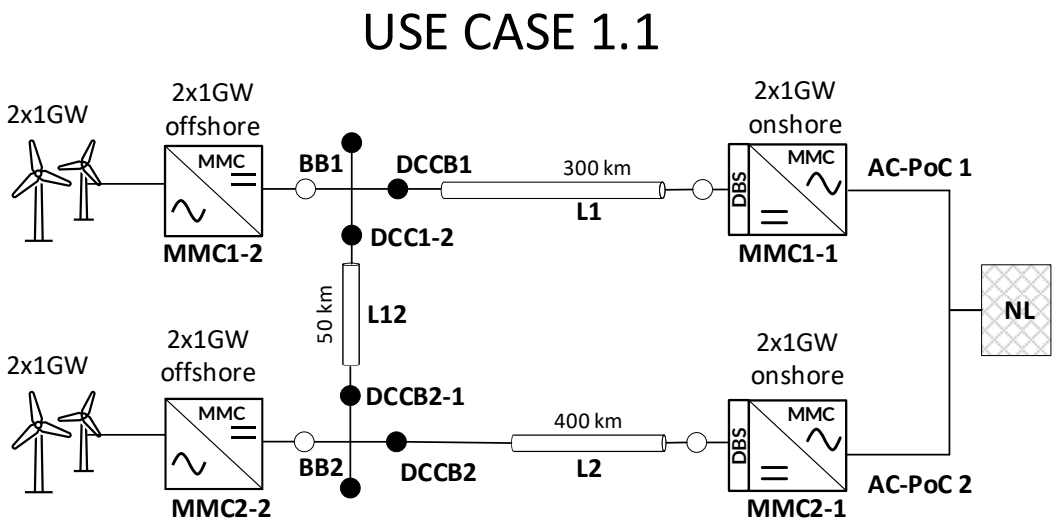


Figure 4: Use case 1.1 with naming convention for the converters, lines, and DC circuit breakers.

A more detailed diagram of the hub and spoke configuration is presented in Figure 5 along with naming conventions for voltage and current.

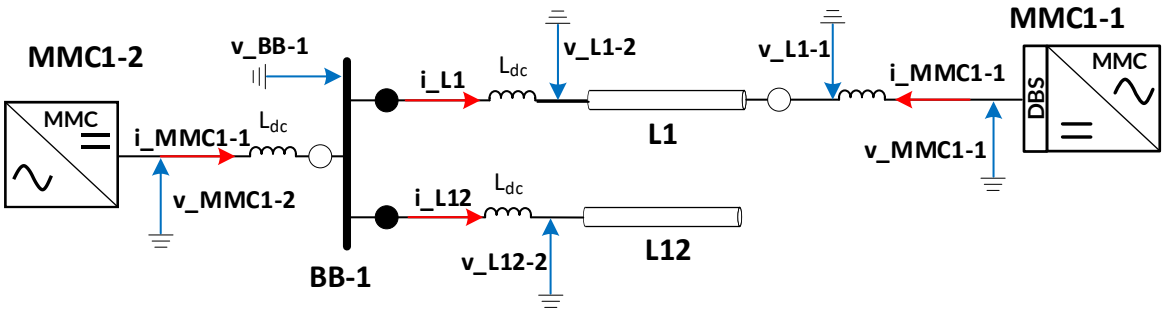


Figure 5: Detailed configuration of a hub with a spoke and an interconnector. The position of the DC inductances, DCCB, as well as location for current and voltage measures (in EMT simulations)

The diagrams of use cases 1.2 & 2 are provided in Figure 7 and Figure 8 along with naming conventions. The offshore windfarm configuration is specified for positive, negative poles and neutral point in Figure 6. This configuration is common to all three use cases.

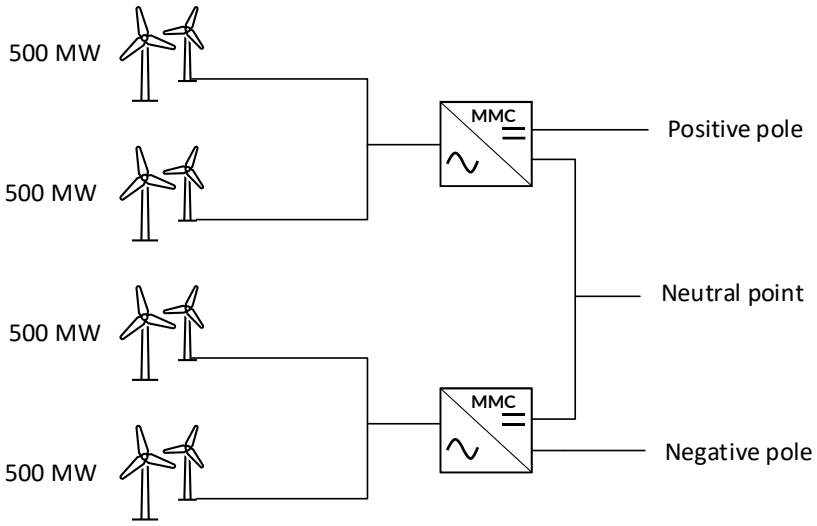


Figure 6: Generic offshore wind farm configuration, common to all use cases

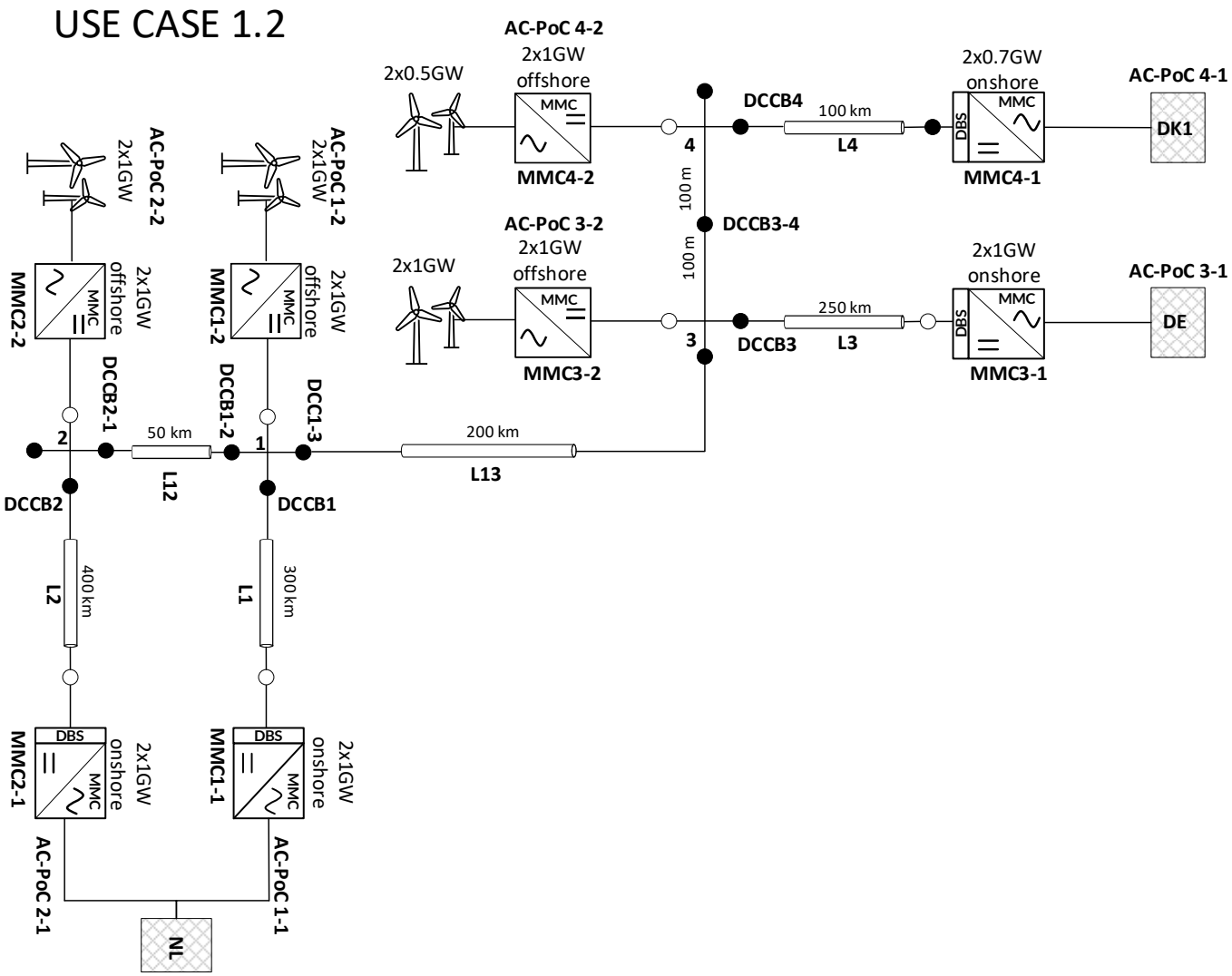


Figure 7: Use case 1.2 with naming convention for the converters, lines, and DC circuit breakers.

USE CASE 2

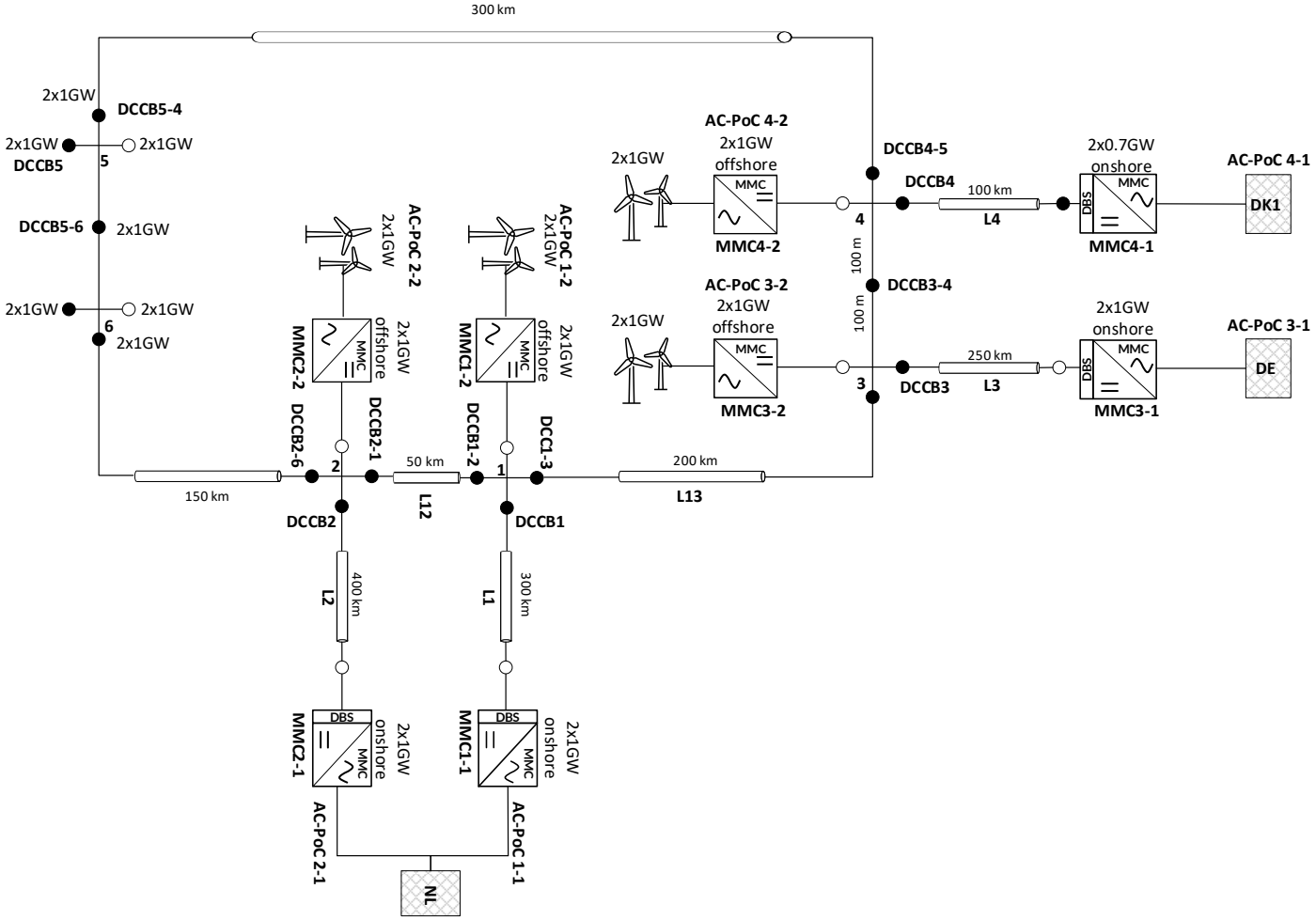


Figure 8: Use case 2 with naming convention for the converters, lines, and DC circuit breakers.

4.3. Input data

A summary of the main input data that have been agreed upon with NSWPH is shown in Table 1. Data followed by a (*) contains the ranges of values used within the study for the sensitivity analyses.

Table 1: Main input data for the project

Input	Parameter	Value	References
Use case and lines lengths	Total length of each line	See section 4.2	NSWPH
HVDC cable	Rated current	1905 A	NSWPH
	Radius of inner solid conductor (m)	30 e-3 m	NSWPH
	Resistivity nuclei/sheath (ohm/m)	nuclei 1.72e-8 Ohm.m sheath 2.83e-8 Ohm.m	NSWPH
	Inner/Outer radius of sheath (m)	inner: 64.5e-3 m outer: 67.5e-3 m	NSWPH
	Outer insulation radius (m)	81e-3 m	NSWPH
	Relative permittivity of 1st & 2nd insulation	2.5	NSWPH
	Cable layout	Bundled cables	NSWPH
DMR cable	Rated current	1905 A	NSWPH
	Radius of inner solid conductor (m)	30 e-3 m	NSWPH
	Resistivity nuclei/sheath (ohm/m)	nuclei 1.72e-8 Ohm.m sheath 2.83e-3 Ohm.m	NSWPH
	Inner/Outer radius of sheath (m)	inner: 48.5e-3 m outer: 52.5e-3 m	NSWPH
	Outer insulation radius (m)	61.5e-3 m	NSWPH
	Relative permittivity of 1st & 2nd insulation	2.5	NSWPH
66kV array cable	Cable distances	10 km	NSWPH
	Rated current	0.73 kA	NSWPH
	Radius of inner solid conductor	0.0149 m	NSWPH
	Resistivity of solid conductor	3.45e-8 Ohm per m	NSWPH
	Relative permeability for solid conductor	1	NSWPH

Input	Parameter	Value	References
	Thickness of 1st insulator	0.009 m	NSWPH
	Relative permittivity for 1st insulator	2.25	NSWPH
	Relative permeability for 1st insulator	1	NSWPH
	Inner semi-conductor layer thickness for Semi-conductor	0.0014 m	NSWPH
	Semi-conductor layers	present	NSWPH
	Outer semi-conductor layer thickness for Semi-conductor	0.0014 m	NSWPH
	Thickness of Sheath conductor	0.002 m	NSWPH
	Resistivity of Sheath conductor	2.2e-7 Ohm per m	NSWPH
	Relative permeability of Sheath conductor	1	NSWPH
	Outer Radius for Inner Insulator	0.069 m	NSWPH
	Relative permittivity for Inner Insulator	2.25	NSWPH
	Relative permeability for Inner Insulator	1	NSWPH
	Outer Radius for Outer Insulator	0.0785 m	NSWPH
	Relative permittivity for Outer Insulator	2.3	NSWPH
	Relative permeability for Outer Insulator	1	NSWPH
	Radius for pipe conductor	0.074 m	NSWPH
	Resistivity for pipe conductor	1.38e-7 Ohm per m	NSWPH
	Relative permeability for pipe conductor	200	NSWPH
	Cable layout	Pipe Type Cable	NSWPH
Substation	HVDC station power	2GW per bipole and	NSWPH

Input	Parameter	Value	References
		1.4 GW per bipole	
	Configuration	Bipole with DMR	NSWPH
Grounding System	Ground connection of the neutral	Solid connection at one terminal (or via a ground resistance up to 15-20 Ohm) and Surge Arrester connection for the other stations.	See SoW A report
MMC parameters	Number of SM per arm	278	NSWPH
	Larm	0.15 pu	NSWPH
	Ceq	145 µF 290 µF 725 µF	SGI
	Csm	6.71 mF 13.5 mF 33.5 mF	SGI
	Energy MMC (Emmc)	20 MJ 40 MJ 100 MJ	SGI
	AC transformer data (offshore transformer).	2x three-phase transformer, 66kV (Y) / 300kV (Δ) – 525 MVA (per Pole)	NSWPH
	AC transformer data (onshore transformer).	3x single-phase transformer, 400 kV (Y) grid side / 300kV (D) converter side – 350 MVA (per Pole)	NSWPH
	Transformer reactor	15 %	NSWPH
MMC control & protection	Current loops* (response time)	3 ms to 5 ms/ a response time of ~3 ms has been used for simulations with use cases.	SGI
	Power loops* (response time)	100 ms to 200 ms/ a response time of 200 ms has been used for simulations with use cases.	SGI
	DC voltage loop* (response time)	30 ms to 100 ms/ a response time of 40 ms has been used for simulations with use cases.	SGI
	Blocking criteria Idc	See section 7.2.1	SGI
	Blocking criteria Vdc	See section 7.2.2	SGI
DCCB	Operating time*	2 ms to 10 ms	SGI
	Breaking capability*	10 kA to 20 kA	SGI
	TIV*	1.5 pu to 1.7 pu	SGI

Input	Parameter	Value	References
DC Protection	DCR*	0 mH to 800 mH	SGI
	Fault identification time*	0.5 ms to 3 ms	SGI
	Breaker failure detection*	0 ms to 2 ms	SGI
OWF parameters	Power rating	500 MVA	NSWPH
	AC voltage rating	66 kV	NSWPH
	AC Transformer	three-phase transformer, 0.6 kV (D) WT side / 66 kV (Y) collector side	NSWPH
	Transformer reactor	0.075 pu	NSWPH
	Ceq at the DC bus	40 mF	NSWPH
	DC chopper Resistor	0.9 Ohm	NSWPH
OWF control & protection	AC current (Maximum)	Id= 1.1 pu / Iq= 0.5 pu	NSWPH
	AC Undervoltage/ Overvoltage criteria	0.3 / 1.3 pu	NSWPH
	DC chopper protection criteria	1.15 / 1.05 pu	NSWPH
	Over/under frequency criteria	55 / 45 Hz	NSWPH
	Maximum Increase of power rate	0.2 pu/s	NSWPH
	Maximum decrease of power rate	0.2 pu/s	NSWPH
Onshore AC side	Short Circuit Level (SCL) Germany and the Netherlands	43.65 GVA	NSWPH
	Short Circuit Level (SCL) Denmark	Min 10 GVA Max 33 GVA	NSWPH
FCR	Continental	3000 MW	NSWPH
FRR	Denmark	700 MW (Higher FRR can be provided by sharing FRR of nearby countries)	NSWPH
	Germany	1400 MW	NSWPH
	The Netherlands	1000 MW	NSWPH

5. Model Development

The development of Simplistic Test Benchmarks (STB) for the different building blocks requires the development of elementary “bricks” which can accurately represent the dynamics of the detailed models that are implemented in the use case. These bricks will be introduced and validated against detailed models in the following sub-sections. The bricks will further serve to build up different STB models for functional requirement and parameter range specification.

5.1. Cable model

This study focuses on a bipolar HVDC configuration with Dedicated Metallic Return (DMR). Thus, one HVDC link consisting of two high-voltage cables (±525kV) and a medium-voltage cable for the DMR are considered. The bundled layout as shown in Figure 9 with dedicated geometry parameters as listed in section 4.3 are chosen. The screen is grounded at each cable end.

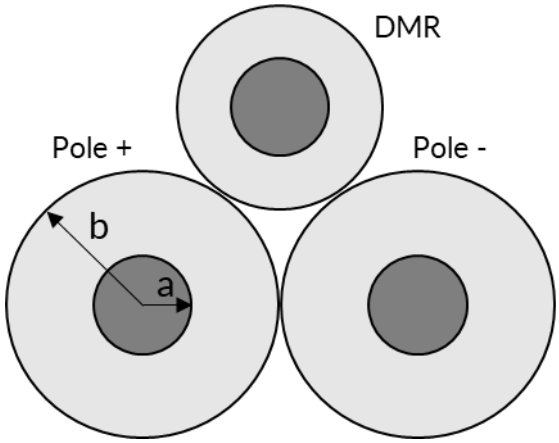


Figure 9 Bipolar HVDC cable configuration with DMR

Nowadays, wideband models or frequency-dependent models are commonly used to represent fast transients in HVDC systems and to consider the frequency dependency of the cable. Such models allow to accurately represent traveling waves related to fault events and switching transients. The major drawbacks of frequency-dependent cable models are the model complexity and the relatively high calculation effort in simulation environments which may impose a small simulation time step in case of short cable sections. Frequency-dependent cable models can be approximated by cascaded pi-sections with multiple parallel RL branches as shown in Figure 10. An increasing number of cascaded elements leads to an increasing approximation of traveling wave behavior, whereas each parallel RL element represents the resistive and inductive value for a given frequency [6]. Capacitive elements are frequency independent.

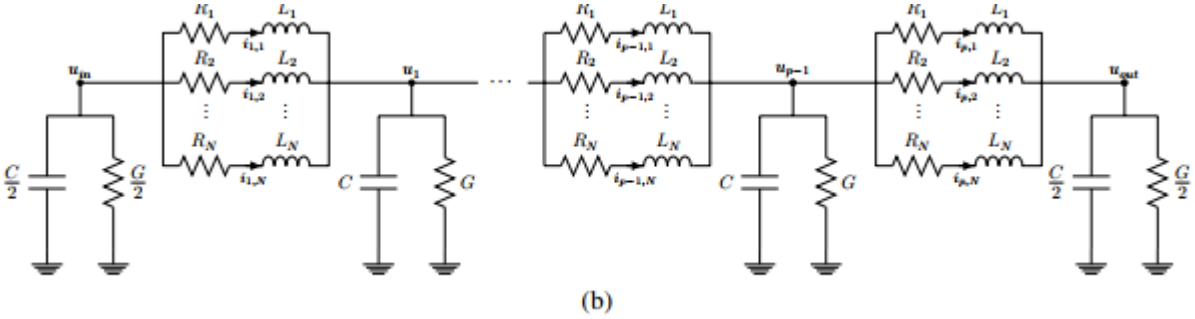


Figure 10 Cascaded pi-model with multiple RL branches in parallel [6]

Some assumptions allow to reduce the complexity of the cable model:

- The mutual coupling of cable pole conductors is negligible due to the grounding of the screen at each end. This implies that any transient event on one conductor will not provoke transients on the other conductors. Therefore, the simplified cable model can be reduced to a single-pole representation wherever other poles are not directly involved.

- In the context of this study, a fully selective fault clearing approach is imposed and the converters are in general not allowed to block except for some specific fault scenarios. This creates a high necessity of DC reactors at each cable end and at each converter output. In the context of cable modeling requirements, DC reactors act as a filter of high transients and smoothens the current largely to one dominant frequency (several hundreds of Hertz). Considering this, the cable model can be further simplified such that cascaded pi-elements and multiple parallel RL branches for multi-frequency representation are not necessarily required.

Based on the above listed simplifications, a simplistic cable model with DC reactors L_{dc} at each end as shown in Figure 11 can be proposed. This adapted pi-model consists of capacitors at each end and two parallel RL branches.

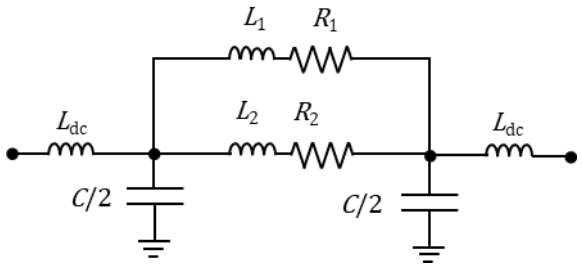


Figure 11 Simplistic cable model for transient and dynamic studies

The parameters can be determined as follows. The lineic capacitance C' is by nature not frequency dependent and can be calculated based on the following equation (a and b indicated in Figure 9).

$$C' = \frac{2\pi\varepsilon}{ln\left(\frac{b}{a}\right)}$$

The parameters of the first RL branch R_1 and L_1 are tuned to accurately represent the first resonance frequency in the Bode plot without DC reactors. The first resonance frequency remains accurately represented when adding DC reactors at the cable end (see Figure 12). After the first resonance frequency, the magnitude is exponentially increasing so that significant damping can be expected. The resistance R_2 of the second RL branch

is tuned such that the overall lineic resistance corresponds to the DC resistance of the wideband model (R'_{dc}=6.09mΩ/km). In this way, the cable model accurately represents the steady state.

$$R'_{dc} = \frac{R_1 R_2}{R_1 + R_2}$$

The lineic parameters are listed in Table 2.

Table 2 Lineic parameters of simplistic cable model

Parameter	Unit	Value
C'	µF/km	0.181
R1'	mΩ/km	45
R2'	mΩ/km	6.923
L1'	mH/km	0.135
L2'	mH/km	1.5

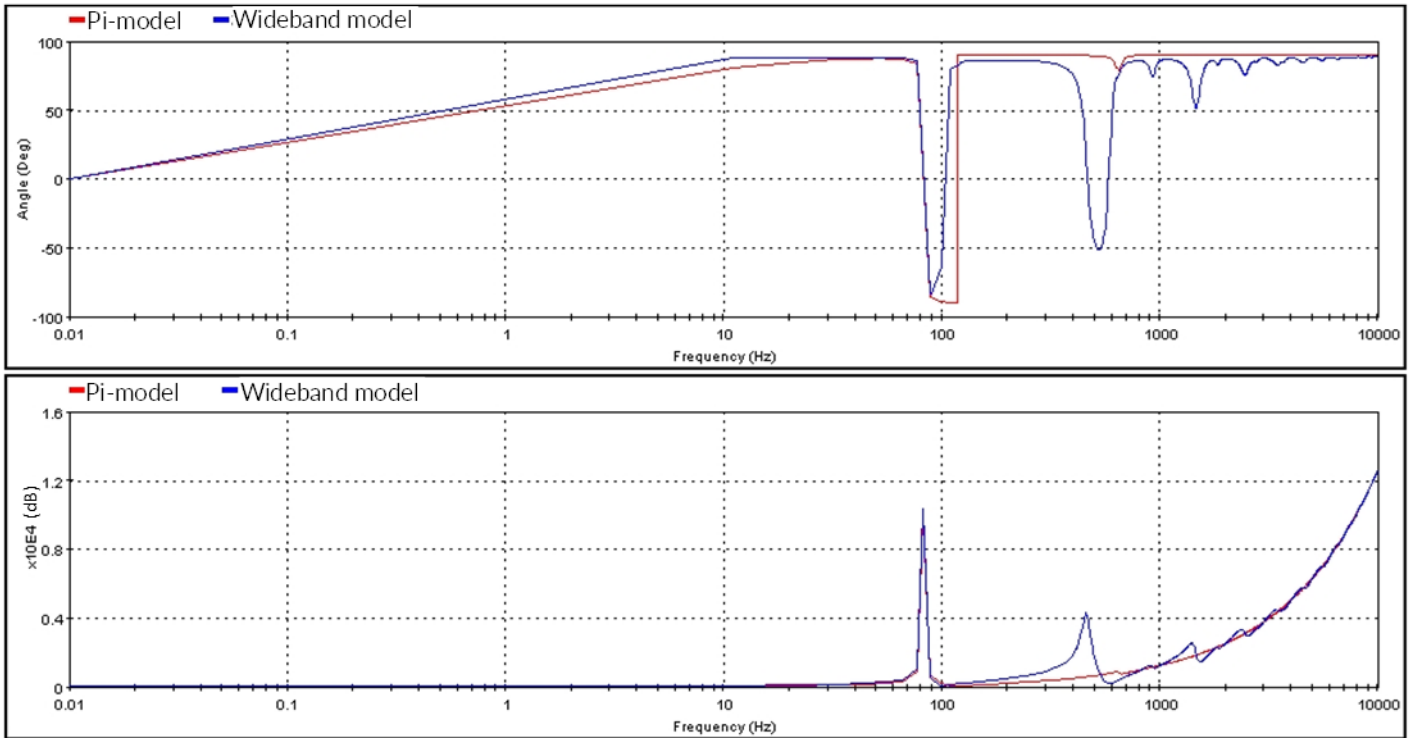


Figure 12 Bode plot (upper plot: angle, lower plot: Magnitude) of 100km cable with DC inductors of 200mH at each end; blue: Wideband model, red: proposed simplistic cable model

Figure 14 and Figure 15 show respectively the dynamic current and voltage response of the simplistic cable model compared to the wideband model (Test configuration, see Figure 13). The comparison is shown for different cable lengths (50km, 200km) and different DC inductors (100mH, 300mH).

From the results, it can be concluded that the proposed simplistic cable model accurately represents the current and voltage evolution during transient events. Both the frequency and the peak value of the oscillation are well represented. However, it should be noted that for long cables (>200km), the propagation time becomes long which leads basically to an additional delay to be considered [7] [8]. For the simplified cable model, this can be adjusted by adding a pi-section in series. Taking a total cable distance of 400km as an example, this would imply for the simplified model to use two sections of 200km each.

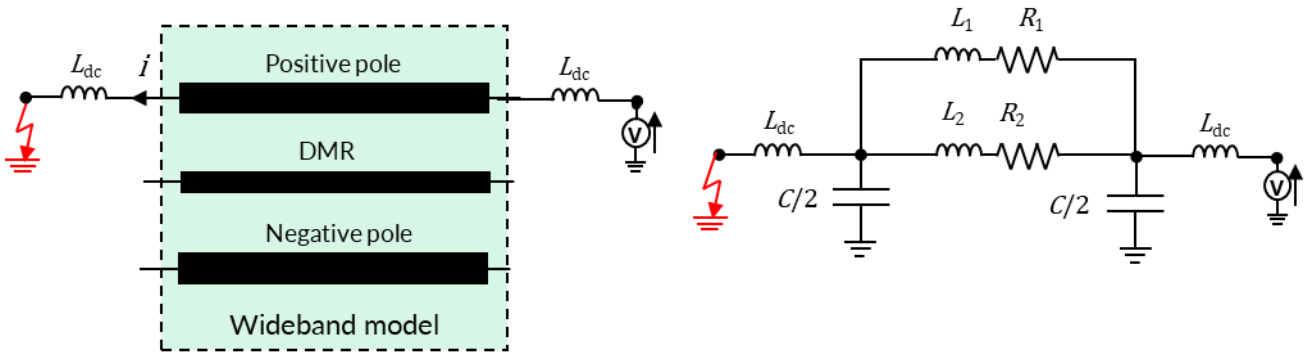


Figure 13 Test circuit for comparison of dynamic response of wideband model (left) and pi-model (right)

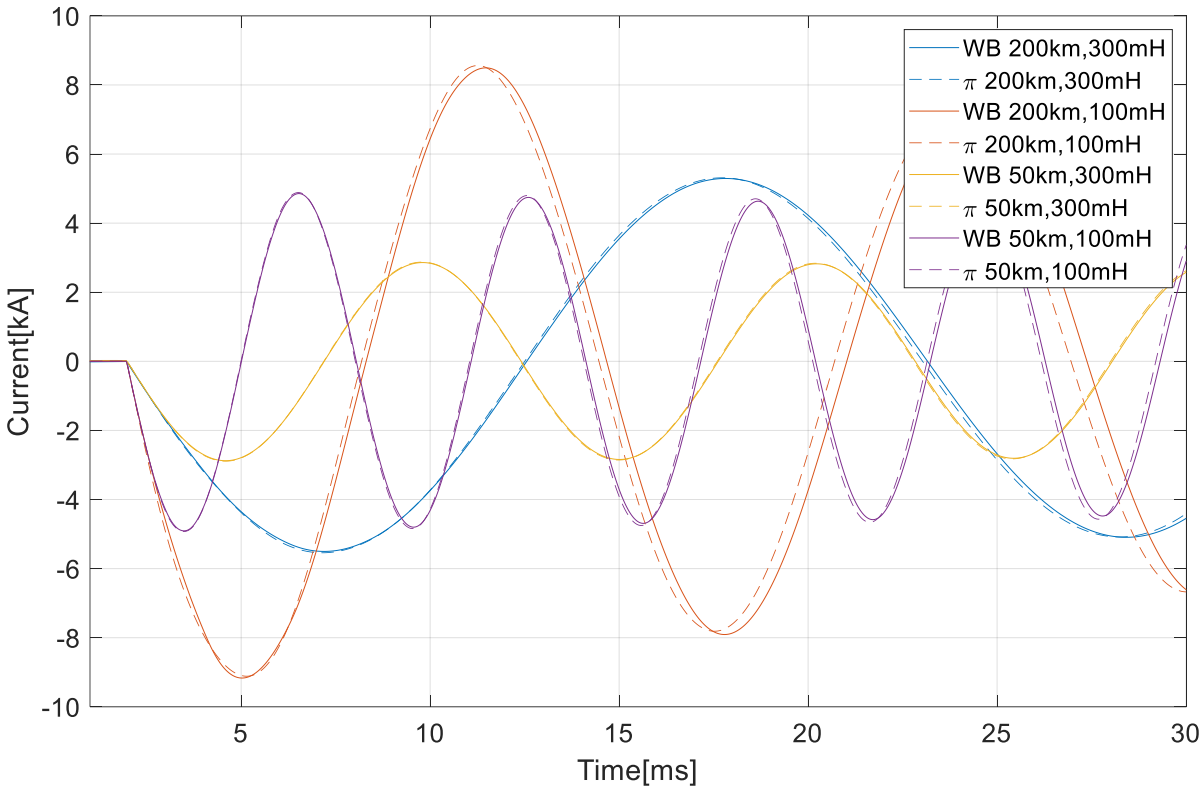


Figure 14 Discharge test of cable; Comparison of current response of wideband model (solid) and pi-model (dotted) for different cable length and DC reactors

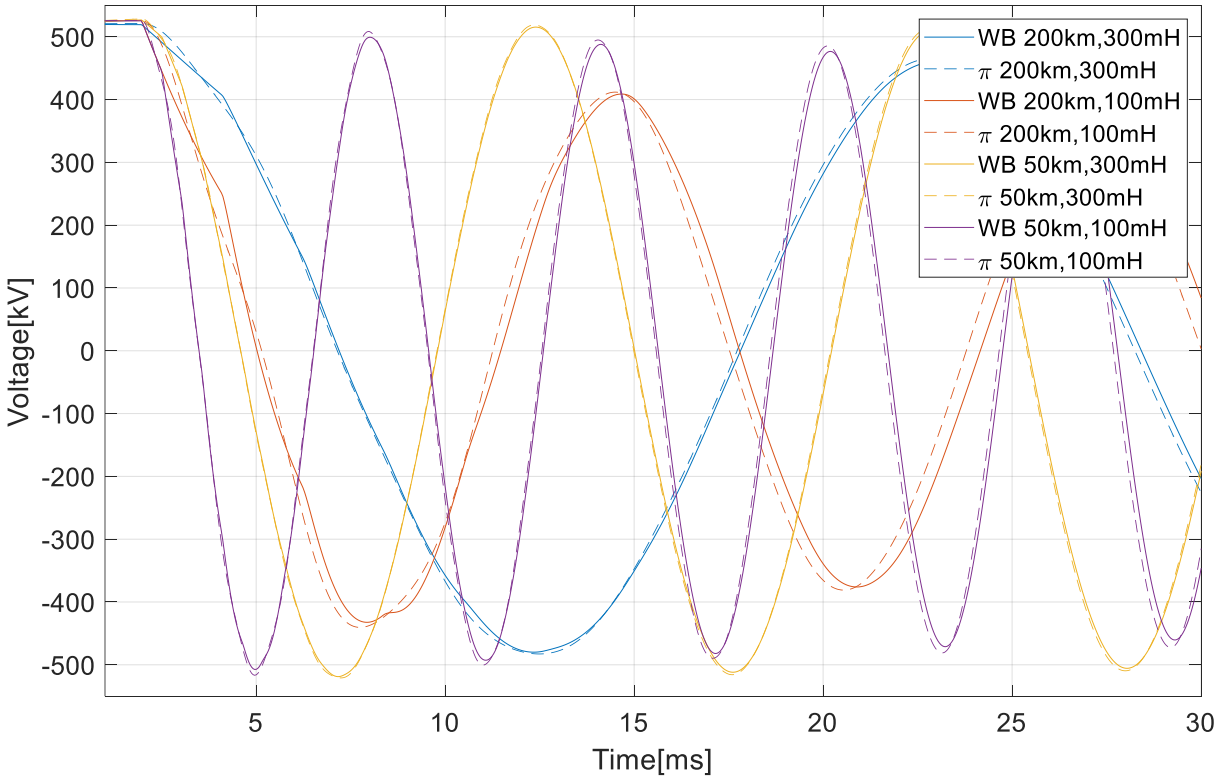


Figure 15 Discharge test of cable; Comparison of voltage response of wideband model (solid) and pi-model (dotted) for different cable length and DC reactors

5.2. AVM model AC/DC

An MMC consists of a large number of switching devices. Depending on the type of studies and phenomena of interest to be analyzed, a certain simplification is commonly made. The CIGRE technical brochure 604 "Guide for the development of models for HVDC Converters in a HVDC Grid" summarizes the definitions of 7 different types of computational models, among which two types are commonly used for EMT simulations of HVDC system performance studies. Further clarification has been made in [9].

Two principal modelling methods commonly used in the literature are shown in Figure 16.

The Average Arm Model (AAM) representation is illustrated in Figure 16.a. This model assumes that the MMC arms consist of a sufficiently large number of submodules (SMs) and that the voltages of all the SMs capacitors are maintained within a close range by an appropriate Balancing Control Algorithm (BCA). Each MMC arm can be then represented with sufficient accuracy by an equivalent arm capacitor that is charged and discharged by the power exchange between the arm and the AC/DC grids. The validity of this model for accurately reproducing the dynamics of both the AC and DC grids interfaced by the MMC, as well as the dynamics of the internal circulating currents has been verified by simulations and experiments in several existing articles [10]. This model is widely used for development and validation for inner current loops such as AC current controllers or the circulating current suppression controllers. For those reasons, this model is used as a reference to verify the accuracy of the model applying further simplifications presented in the following.

Further simplifications can be made for the design and tuning of high-level control systems such as the regulation of the voltage of the DC grid. The so-called Average Value Model (AVM) model for AC/DC system studies is depicted in Figure 16.b. The average response of the MMC on the AC and DC side at the connection point is modeled separately, and the energy conversion between AC and DC is assumed to be an ideal power conversion. For the AC side, the MMC behavior is represented by using controlled voltage sources, which follow the AC voltage setpoint generated by the inner control loop. On the other hand, the DC side behavior of the MMC is represented by a controlled current source connected in parallel with an equivalent capacitor of the MMC. The DC current is derived by dividing the AC power output by the DC voltage, based on the ideal power conversion principle. The losses inside the converter, which are generally around 1% [11], are represented by the resistance on the DC side. However, it should be noted that, in practice, these losses depend on the switching frequency and the modulation technique, as well as the currents which circulate through the converter arms. Those are simplified in the AVM model.

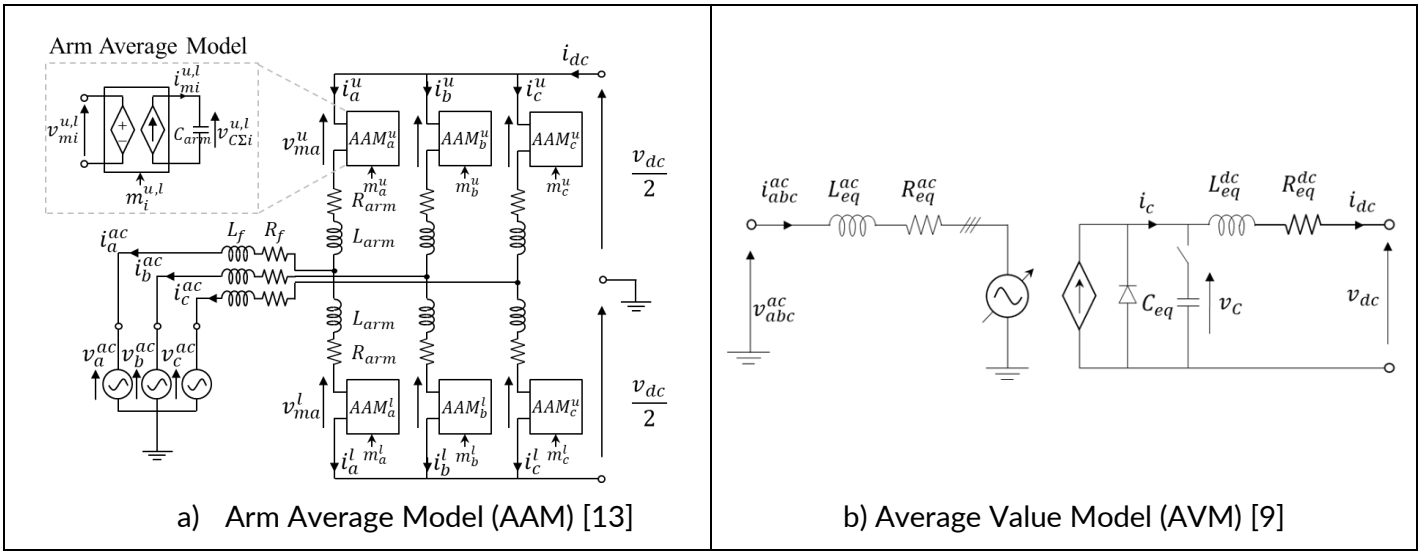
The equivalent arm capacitors seen in the previously mentioned AAM model are further aggregated into the single equivalent capacitor C_{eq}, whose size is derived from the energy conservation principle [12]:

$$E_{mmc} = 6N_{SM}\left(\frac{1}{2}C_{SM}V_{SM}^2\right) = 6\frac{1}{2}C_{arm}(N_{SM}V_{SM})^2 = \frac{1}{2}C_{eq}(N_{SM}V_{SM})^2$$

$$C_{eq} = 6C_{arm}.$$

This aggregation inevitably makes the behavior of each converter arm indistinguishable and simplifies the phenomena that stem from the interactions between them.

In summary, while the AAM model represents the internal dynamics of the MMC with 11 independent state variables (5 converter arm currents and 6 arm capacitors), the AVM has only 4 independent internal states, namely the two AC currents (two AC phase currents in balanced three-phase AC system, or alternatively dq components), the DC current, and the equivalent internal capacitor voltage.



a) Arm Average Model (AAM) [13]

b) Average Value Model (AVM) [9]

Figure 16 MMC equivalent representations based on two types of modelling methods

The simplification of the converter model also entails a simplification of the control system at the same time. In Figure 17 and Figure 18, the high-level view of the MMC controller implemented in the PSCAD use case simulation models and simplified control scheme adapted for the AVM AC/DC are depicted. Since the arm currents are no longer distinguished in the AVM AC/DC model, the Circulating Current Suppression Controller (CCSC), whose role is to suppress the unwanted internal current circulations between the arms, is no longer

applicable and should be removed. However, the AC current controllers as well as the superior outer control loops connected above can be applied without change.

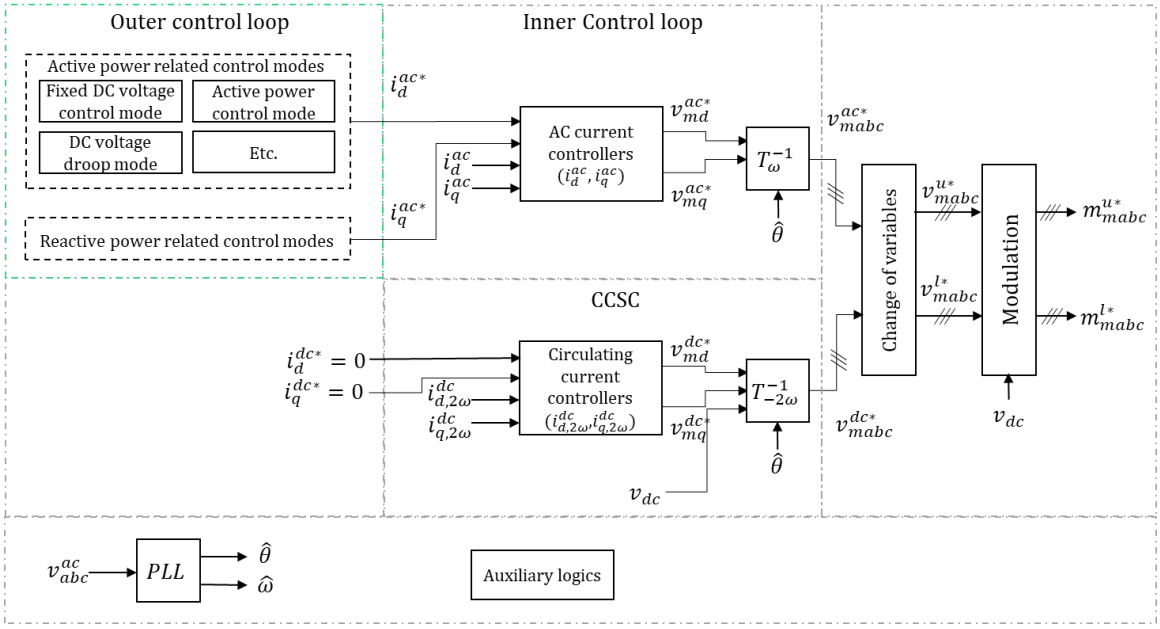


Figure 17 High level view of the MMC controller implemented in the PSCAD Use case

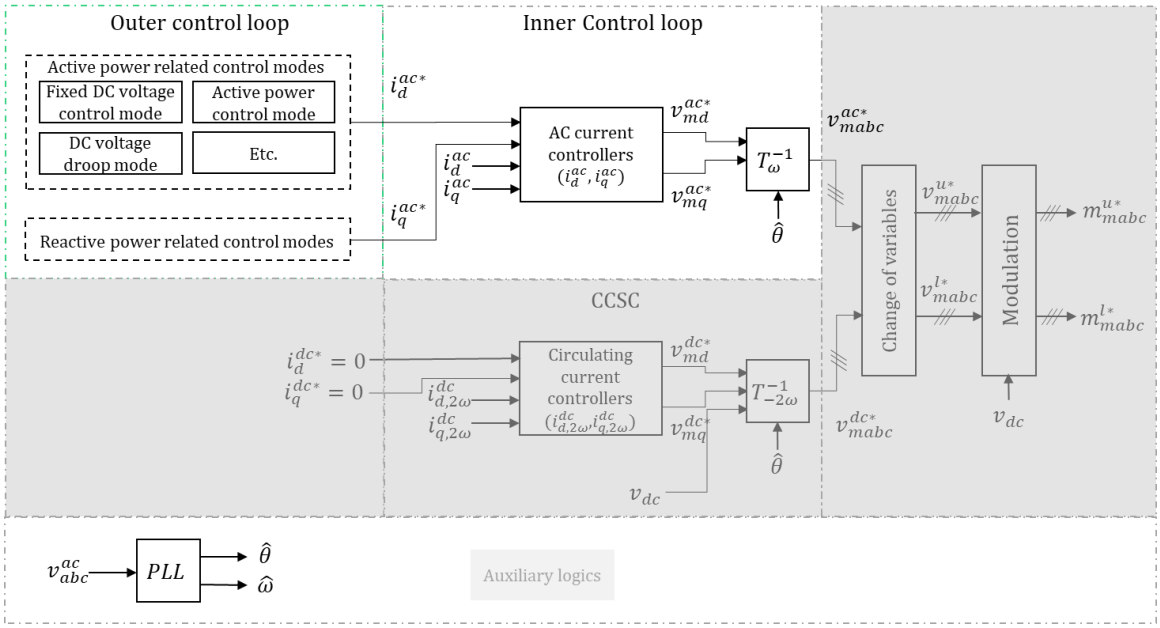


Figure 18 Simplified control scheme adapted for AVM AC/DC model

5.2.1. Validation of AVM model AC/DC

In order to confirm the accuracy of the behavior of the developed AVM model and to demonstrate the extent to which this model is valid, comparative studies against the AAM model were performed. In the reference

AAM case, the provided control system and parameters in Table 1 are used, and in the AVM, which is the subject of the verification, the same parameters as in the AAM case are assigned. The simulations for verification were conducted in two phases. First, a set of comparative tests of the converter station alone were performed (Phase 1). The test was performed in each of the three principal control modes: Phase1-A: fixed active power control mode; Phase1-B: fixed DC voltage control mode; and Phase1-C: DC voltage droop control mode. In Phase 2, in order to verify the validity of the AVM model in MTDC grid simulations, in addition to the AVM models, the simplified cable models described in Section 5.1 were used to represent a given use case. Then, the results were compared against the ones obtained from the detailed model.

5.2.1.1. Phase 1: Validation of the station alone

Figure 19 depicts the simulation setup. The MMC station is interfaced with a voltage source on the AC side. On the other hand, the DC side configuration depends on the type of study and is determined by the position of the switch (*sw*) at 1 or 2, as summarized in Table 3. The size of the DCR installed on the DC side terminal of the station was fixed to 200 mH. The capacitor, which represents the external system on the DC side of the MMC station, C_l is set to 300 µF. The disturbance scenario was determined according to the purpose of the verification.

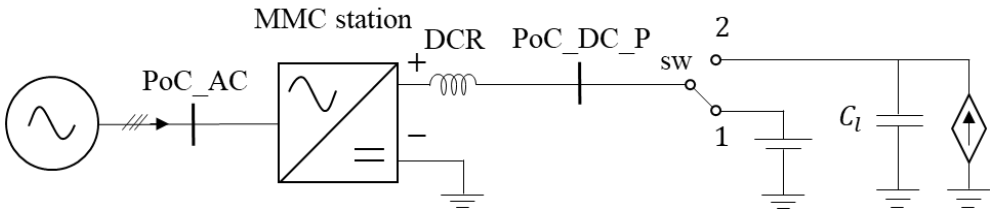


Figure 19 Simulation setup for validation of the station alone

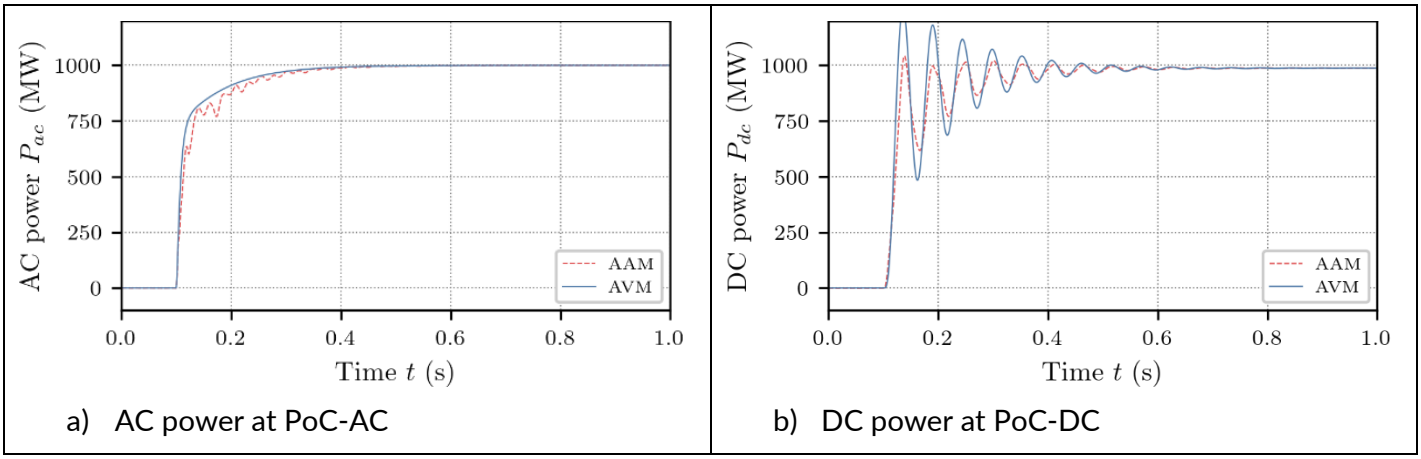
Table 3 Switch position for each study case

Study case	Switch position
(a) Fixed active power control mode	1
(b) Fixed DC voltage control mode	2
(c) DC voltage droop control mode	2

(a) Fixed active power control mode

For this study, the DC side switch *sw* was set to 1, i.e. ideal DC voltage source. The MMC station was set to the fixed power control mode. At t=0.1s, the set-point of the active power was changed from 0 to 1000 MW. The obtained results are compared in Figure 20. The dashed red line shows the results obtained from the MMC station model in the use case, where the MMC is represented using the AAM, while the blue line is the result obtained from the developed simplistic model using AVM. Figure 20a shows the active power response. As expected, the active power output follows the set-point change and reaches the new set-point value promptly. Some small power fluctuations observed in the detailed case are not seen in the simplified case based on AVM, but the dominant dynamics are quite accurately reproduced. Figure 20b shows the DC power measured at the

PoC-DC of the station. It is observed that DC power dynamics has a slight difference in the magnitude of the oscillation component. This may be due to the fact that the energy exchange that occurs between the six converter arms is neglected in the AVM and that the control of the circulating current is omitted also in the AVM, resulting in a difference in the damping of this frequency. Note that both show good agreement in the steady-state values.



a) AC power at PoC-AC

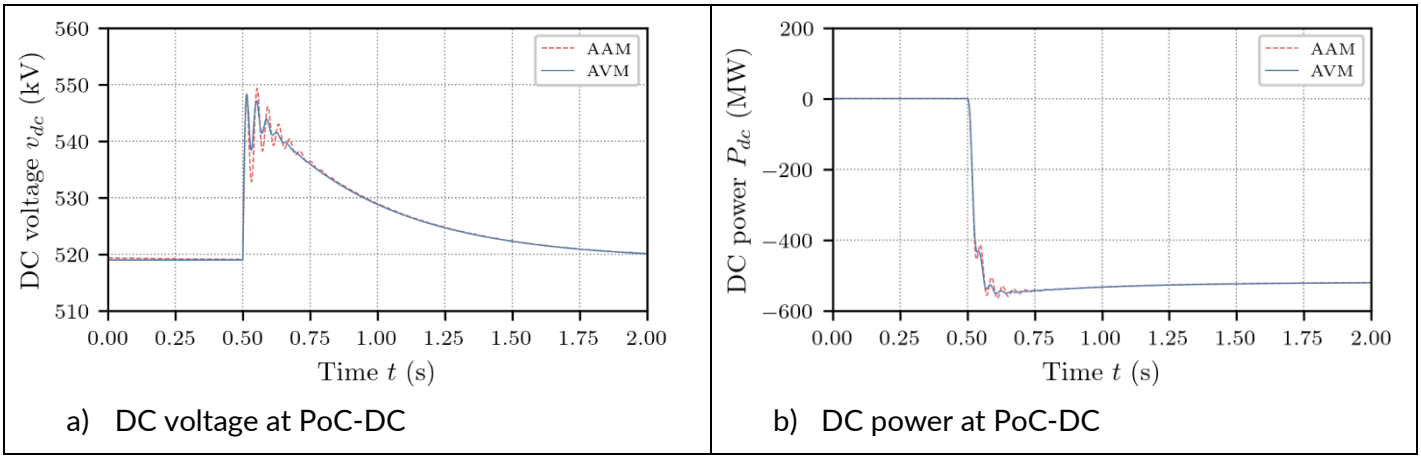
b) DC power at PoC-DC

Figure 20 Comparison of the obtained results - Phase1-A: Fixed active power control mode.

(b) Fixed DC voltage control mode

For this verification test, the DC side configuration is set with *sw* at 2, so the converter station is connected to the controlled current source with a capacitor. The operating mode of the converter is set to fixed DC voltage control mode. At t=0.5s, a 1kA step current injection is generated by the current source. Then, for both models, the response of the converter to the disturbance was observed.

In Figure 21, the results obtained with the detailed model and the simplified model are compared. Figure 21a shows the DC voltage. As seen, the simplified model using AVM well represents the dominant DC voltage dynamics. In Figure 21b, the DC power measured at PoC-DC in each case is shown. It can be seen that the response speed and amplitude of the two models are in very good agreement.



a) DC voltage at PoC-DC

b) DC power at PoC-DC

Figure 21 Comparison of the obtained results - Phase1-B Fixed DC voltage control mode.

(c) DC voltage droop control mode

Finally, this study intends to verify whether the simplified model can reproduce the behavior of the droop control mode in response to an external disturbance, which is vitally important in the voltage control of MTDC grids. The same DC side configuration as (b) Fixed DC voltage control mode, i.e., $sw = 2$, as well as the same disturbance scenario was considered here. For the test of the droop control mode, the same droop controller scheme implemented in the reference case was implemented into the simplified model. The same droop gain of 5% is assigned for both models.

Figure 22 shows the obtained results. In Figure 22a, the obtained DC voltages are compared. Like the previous study on the Fixed DC voltage control mode, the simplified model well reproduces the DC voltage dynamics. In Figure 22.b and c, the DC and AC power are shown. For these two figures, the differences between the two models are even smaller than those observed in the DC voltage and power. Finally, Figure 22d shows the DC current, which shows sufficiently accuracy.

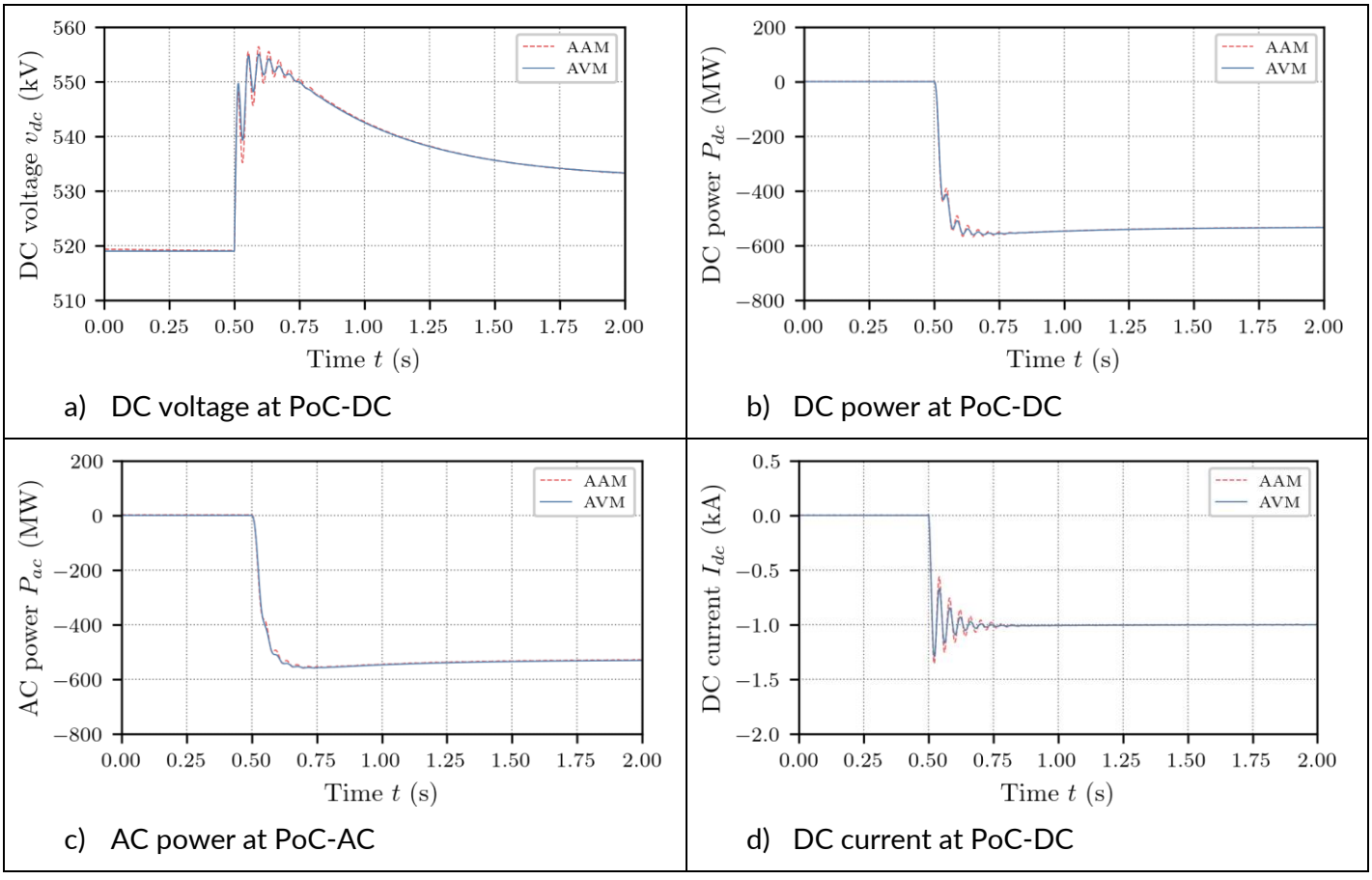


Figure 22 Comparison of the obtained results - Phase1-B DC voltage droop control mode

These verifications demonstrated that the simplified MMC station model with AVM can accurately reproduce the dominant dynamics of the detailed station model with AAM and in all the three principal control modes.

5.2.1.2. Phase 2: Validation in an MTDC grid

In the previous section, it was confirmed that the simplified model using the AVM model can well reproduce the behavior of a single MMC station. This section is intended to verify whether the model can also reproduce well the behavior of MTDC grids. For this purpose, the MTDC grid given as use case 1.1 (recalled and shown in

Figure 23) was constructed using the developed simplified models. Then, it is verified by simulations whether the simplified MTDC grid model exhibits the same behavior as the detailed MTDC grid model.

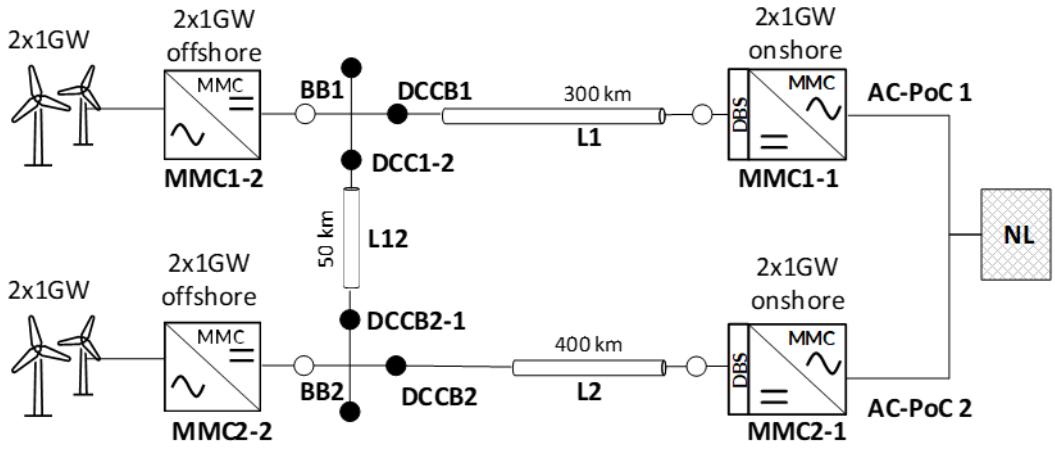


Figure 23 Use case 1.1

Figure 24 shows the overview of the simplistic testbench replicating the use case 1.1. It consists of only the simplified models; the MMC station models using AVM validated in the previous simulations, and simplified cable models described in Section 5.1. In general, an offshore AC/DC converter station connected to a wind farm absorbs the power from the wind farm by solid grid forming control (fixed AC voltage and frequency control mode) and thus has no control over the active power injection by the AC/DC converter station itself. However, this feature of the solid grid forming control is currently not considered in the developed AVM AC/DC model. In other words, the offshore converter station and the wind farm as a whole can be considered as a converter working in the active power control mode. Therefore, the offshore wind farm is represented here by a converter working in the active power control mode.

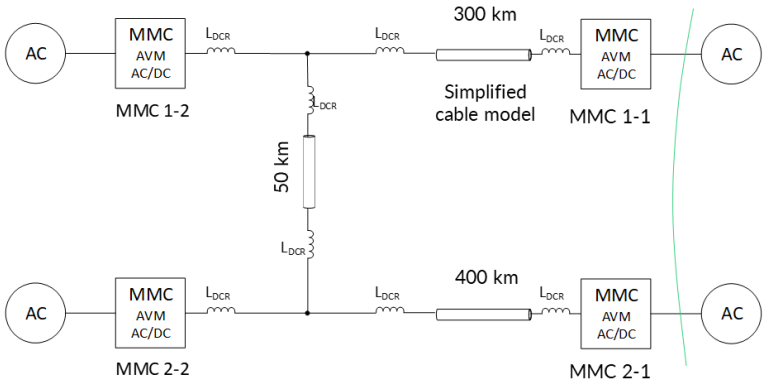


Figure 24 Overview of the simplistic test benchmark (Use case 1.1)

Here, both static and dynamic aspects are subject to validation. The initial set-points are given in Table 4:

Table 4 Initial operational set-points

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain s [%]
MMC 1-1	Vdc droop control	-485	519.5	5
MMC 1-2	Fixed AC power	+700	N/A	N/A
MMC 2-1	Vdc droop control	-485	519.5	5
MMC 2-2	Fixed Ac power	+300	N/A	N/A

The convention of designating a positive sign the power injected into the DC grid is used. Onshore stations MMC 1-1 and 2-1 are in Vdc droop control mode, which are responsible for regulating the DC voltage.

(a) Validation in steady state

In Figure 25, the comparison of the results obtained from the detailed use case simulation model (UC: use case, shown in dashed line) and the simplistic test benchmark (STB, shown in solid line) are summarized. In Figure 25.a, the DC voltages at PoC-DCs of the stations are compared. The steady-state oscillations seen in the case of UC are not observed in STB, but STB accurately takes the average values of the oscillations. Figure 25.b-d show the AC power, DC power, and DC current at PoC, respectively. No visible difference can be observed. In Figure 25e and f, the power and current of the cables are depicted. Similar to the PoC, no visible difference can be seen between the two models.

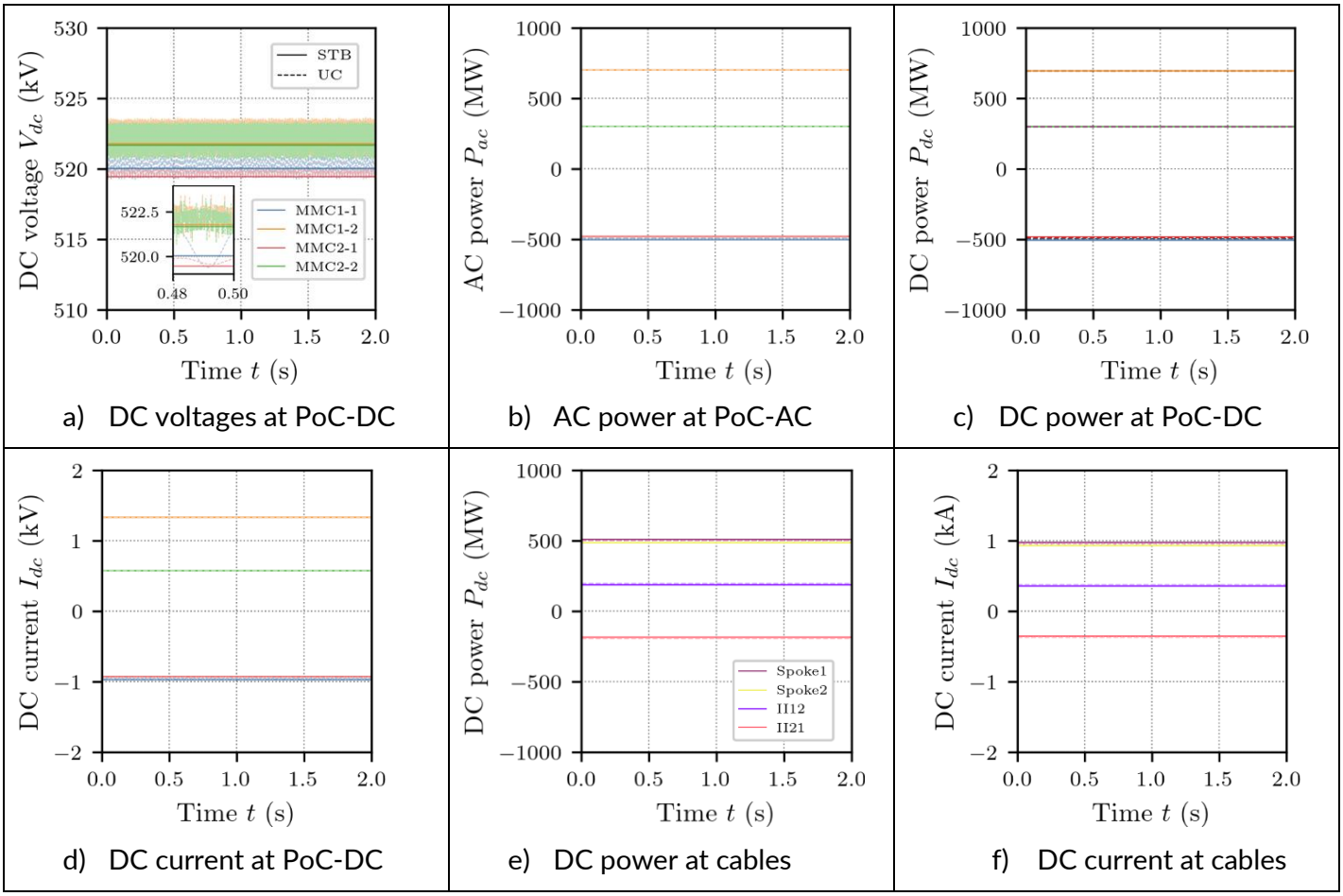


Figure 25 Comparison of the obtained results – Phase2-A Validation under steady-state (Solid lines show the results obtained from the developed STB, whereas the dashed lines show the results obtained from the detailed UC. The figures a) to d) shows the measurement at AC/DC converter stations with the colors indicated in a), whereas the figures e) and f) show the measurements at lines with the colors indicated in e))

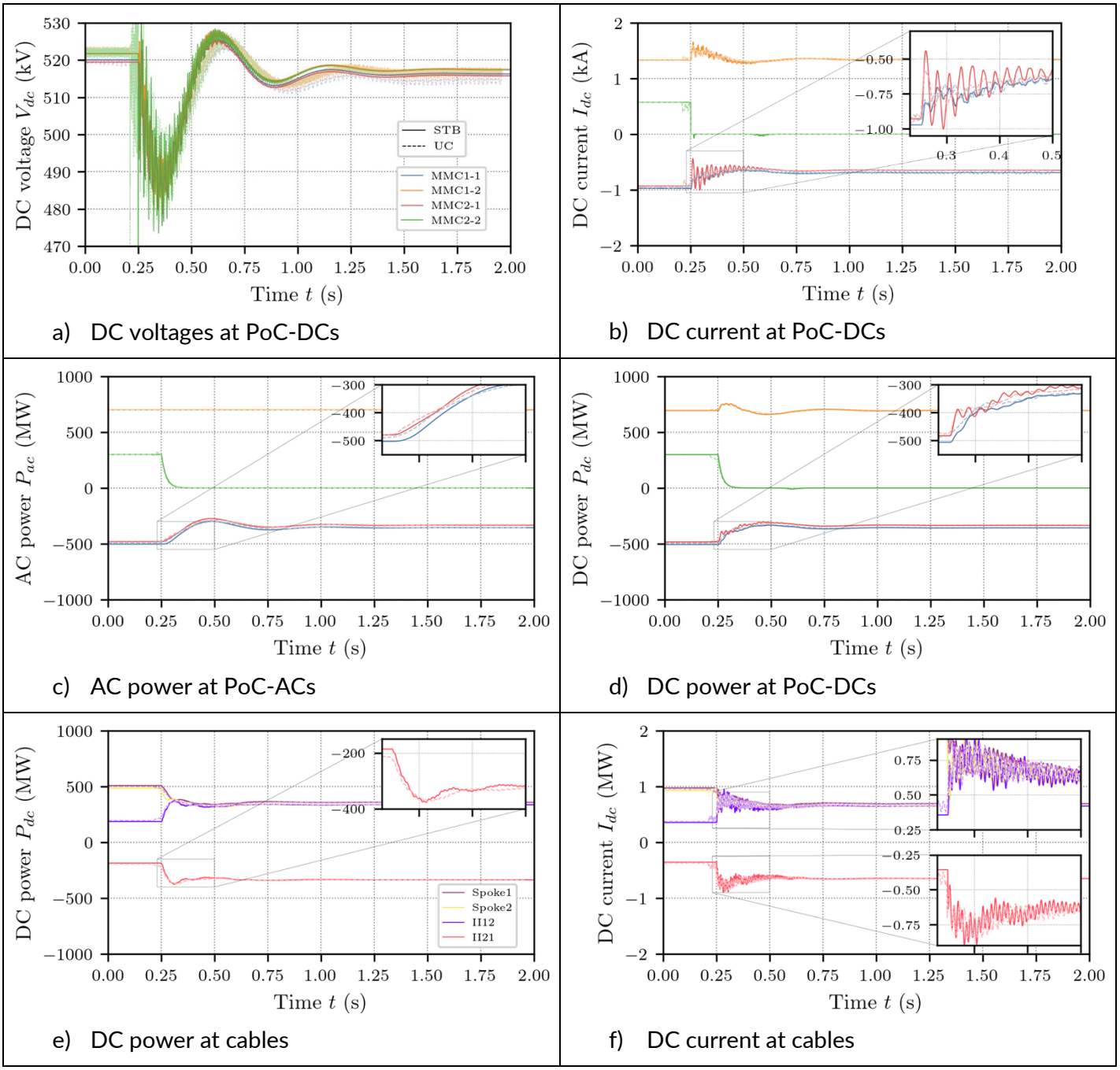
(b) Validation of dynamic behavior

Using the same setup and parameters, this section examines the dynamic behavior to confirm the validity of the test benchmark for the use of system level control design studies. To this end, at t=0.25s, MMC2-2 is forcefully blocked. This leads to an immediate loss of power injection of 300 MW.

Figure 26 shows the obtained results. Here as well, the UC results are shown in dashed lines and the STB results in solid lines. Figure 26a shows the DC voltages. First, the dynamic behavior of the voltage is well captured. It is observed in both the STB and UC cases that there are fast harmonics after the disturbance, but they are only temporary Figure 26b shows the DC currents. In conjunction with the harmonics observed in the voltages, DC currents also show some fast transient oscillations. It is observed that the STB case shows more pronounced and longer decay of these oscillatory components than the case with UC. However, the dominant dynamics are well produced by the STB. In Figure 26c and d, the power at PoC-AC and DC are shown, respectively. Compared to DC voltage and current, UC and STB show very consistent responses. In Figure 26e and f, the power and currents of cables are shown.

In both cases, the dynamic behavior is captured accurately enough, while DC power has its behavior reproduced more accurately than the DC current. Although the offshore AC/DC converter stations in the STB are represent

in constant power mode, whereas the offshore stations in the detailed UC simulation are in V/f control modes interfaced with wind PPMs, the dynamic behavior obtained by the STB and UC coincide well. The results suggest that the behavior of the offshore AC/DC converter station against DC voltage variations can be well reproduced by the constant power mode. On the other hand, there is a slight difference in the decay speed of relatively high-frequency (30-100 Hz) transient oscillations immediately after the disturbance.



a) DC voltages at PoC-DCs

b) DC current at PoC-DCs

c) AC power at PoC-ACs

d) DC power at PoC-DCs

e) DC power at cables

f) DC current at cables

Figure 26 Comparison of the obtained results – Phase2-B Validation of dynamic behavior (Solid lines show the results obtained from the developed STB, whereas the dashed lines show the results obtained from the detailed UC. The figures a) to d) shows the measurement at AC/DC converter stations with the colors indicated in a), whereas the figures e) and f) show the measurements at lines with the colors indicated in e))

5.2.2. Summary

It was confirmed that the developed AVM AC/DC model of the MMC can sufficiently and in accurate manner reproduce the global system dynamics even in the MTDC grid simulation. However, some discrepancies were still observed. For the proper use of the developed model, the limitations of the model and the suitable conditions for use are summarized in this section.

Any simplification of the model comes with a corresponding cost. Compared to the AAM model, the AVM model has significantly fewer internal state variables. While the AAM model represents the internal dynamics of the MMC with 11 independent state variables, the AVM has only 4 independent internal states. In accordance with the simplification of the internal states, the controllers related to those simplified states have been also removed. Since the state of the entire system at a given instant is determined by these state variables, reducing the number of represented states inevitably involves the neglect of certain internal interactions.

The arm capacitor voltages of the MMC are known to have periodic oscillations at multiple frequencies even in steady state due to the energy exchanges that take place between the six arms and the AC and DC grids. While those non-linearities are well represented in the AAM, where each arm is represented independently, they are not reproduced in the AVM because the six arms are aggregated into one state.

It is also acknowledged that the developed AVM model cannot accurately reproduce the current immediately after blocking, which strongly depends on the voltage potential of each arm. This appears as the difference observed in the decay speed of the fast frequency components (around 30~100 Hz) provoked by the converter blocking.

However, the energy imbalance in the DC grid, appears in the form of the dominant DC grid voltage variation, caused by the loss of power transfer capability due to a converter blocking can be reproduced quite accurately.

In summary, the developed AVM can well reproduce the global behavior of the MTDC grid comprising MMCs, except under blocking. Thus, this is indeed useful for designing and tuning system-level control systems, such as DC voltage droop control, post-contingency active power recovery, in line with the recommendation in [9].

5.3. AVM model DC

The AVM model AC/DC introduced in the previous section takes into account to some extent the AC side and dedicated AC control loops. The model can be further simplified if the focus is on DC fault and protection studies. In fact, the current evolution from fault inception to fault neutralization (terminology from CIGRE TB 683 [14]) lasts in the range of several milliseconds. The fault current contribution of converters is mainly characterized by the submodule capacitor discharge on the DC side, while AC side control loops have a minor impact as their time constants are high compared to fault transients [15]. Considering this, a simplified AVM model, further denoted as "AVM model DC", will be introduced.

5.3.1. Model description

The corresponding Single-Line Diagram (SLD) of the AVM DC model is shown in Figure 27 [15].

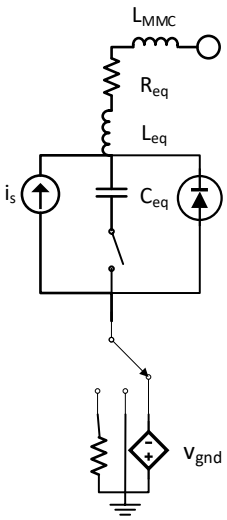


Figure 27 Single line diagram of AVM DC

It consists of an equivalent representation of submodule capacitance C_{eq}, arm inductance L_{eq} and arm resistance R_{eq}. The switch in the branch of the equivalent submodule capacitance is closed in unblocked state and open in blocked state. Even though this model does not represent the AC fault current contribution after blocking, the free-wheeling diode behavior immediately after blocking can still be represented by a bypass of the capacitor. This is needed when investigating backup protection scenarios where the closest converter is allowed to block. The equations for equivalent parameters are provided hereunder. C_{SM} and N_{SM} are respectively the submodule capacitance and the number of submodules per arm. The equivalent arm resistance considers the conduction losses per arm in terms of arm resistance R_{arm} and the number of on state IGBT submodules per arm R_{ON}. Larm is the inductance of each arm.

$$C_{eq} = 6\frac{C_{SM}}{N_{SM}}$$

$$L_{eq} = \frac{2}{3} L_{arm}$$

$$R_{eq} = \frac{2}{3} (R_{arm} + \sum R_{ON})$$

Even though the AC control loops are neglected, a basic power control can still be represented by the following equation, where P*, v_c and i_s are respectively the AC active power reference, the capacitor voltage and the source current. The equation holds under the assumption of a lossless converter and no error of the current controller during steady-state operation [15]. The simplified control scheme allows to consider a pre-fault load flow and its impact on the capacitor discharge.

$$i_s(t) = \frac{P^*}{v_c(t)}$$

Similarly, a simplified voltage control can be implemented. When working in Vdc control, the current injected aims at stabilizing the dc voltage V_{dc} at the reference voltage V_{dc}^*, using a PI controller:

$$I_{DC}(t) = k_p\left(V_{dc}^* - V_{dc}(t)\right) + k_i \int \left(V_{dc}^* - V_{dc}(t)\right) dt$$

where the PI parameters k_p and k_i correspond to the parameter implemented in the full AAM model for the voltage control loop.

The grounding scheme has an impact on the fault current evolution in case of Pole-to-Ground faults. Therefore, different grounding schemes are implemented and can be selected according to the needs:

- → Ideal grounding
- → Resistive grounding (R_{gnd})
- → Surge arrester grounding (v_{gnd})

If a surge arrester grounding is selected and a pole-to-ground fault is applied, the surge arrester conducts the fault current returning by the ground. Hence, the clamping voltage of the surge arrester is activated and acts as a counter voltage to the fault current. Considering this, the non-linear resistance characteristics of the surge arrester can be further simplified by implementing an ideal voltage source v_{gnd} with a voltage rating equal to the clamping voltage of the surge arrester [16].

5.3.2. Model validation

To validate the proposed AVM DC model against the AAM that is implemented in the use case, a PtG fault is applied at the converter output as shown in Figure 28. The fault is applied at T_{fault}=2ms. The results are shown in Figure 29. The AAM model is simulated with surge arrester grounding and blocking is enabled with an arm current limit of $i_{arm,blk}$=2pu. The AVM DC model is simulated with SA grounding option (dashed) and ideal grounding option (dotted) and blocking disabled. It can be observed that the fault current evolution is highly accurate before blocking when identical grounding is considered (comparing solid and dashed). This leads to the conclusion that the ideal voltage source v_{gnd} represents well the surge arrester characteristics under fault (v_{gnd}=30kV in this case). Secondly, it can be observed that the fault current rises faster when ideal grounding is chosen (dotted). This is obvious but important to consider for a proper DC protection equipment sizing as it represents the worst case of fault current evolution. It should be noted that in this example, blocking is disabled for the AVM DC model but enabled for the AAM model. This explains the discontinuous current evolution for AAM model of the use case (solid).

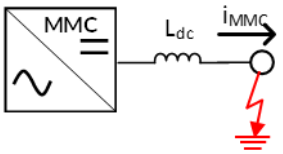


Figure 28 Test scenario 1 for AVM DC model validation

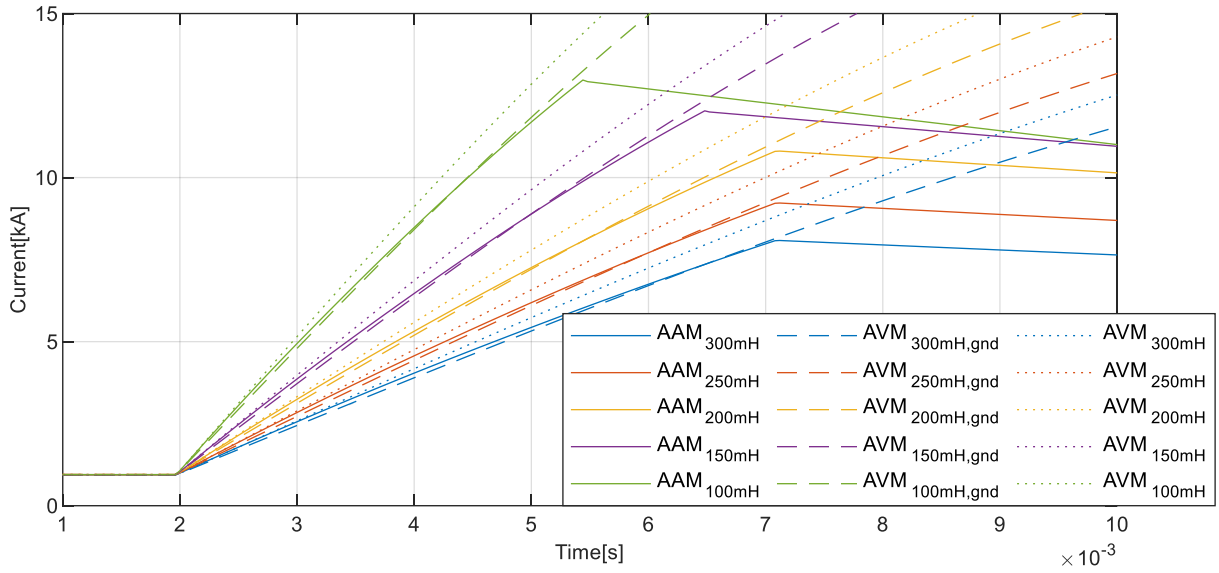


Figure 29 Fault current evolution for PtG fault at converter output with variation of DC reactor L_{dc}; Solid: AAM model with SA grounding, blocking enabled, dashed: AVM DC model considering grounding, blocking disabled, dotted: AVM DC model with ideal grounding, blocking disabled

In test scenario 2, a cable fault is simulated based on detailed models (Averaged arm MMC model from use case in combination with cable wideband model) and simple models (AVM DC model in combination with cable pi-model (see section 5.1)). The fault is applied at 200km and at t=2ms.

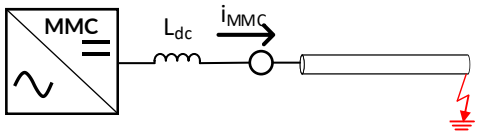


Figure 30 Test scenario 2 for validation of AVM DC model in combination with cable model

Comparing the results of simplistic and detailed models, it can be concluded that the overall fault current evolution is represented with high accuracy. The simple model follows well in amplitude and oscillation frequency which is due to the oscillating behavior of the cable LC-circuit. Comparing in more detail, some slight differences can be observed, for instance in the time between fault occurrence (T=2ms) and arrival of the converter station (T≈3.1ms). The current of detailed model is not increasing until arrival of the first traveling wave (representation of traveling wave behavior in wideband model) whereas for the pi-model the current increases depending on the oscillating frequency of the LC-circuit. It should be noted that for this specific analysis blocking is disabled for both AAM model and AVM model. This is to show the accuracy in pre-blocked state.

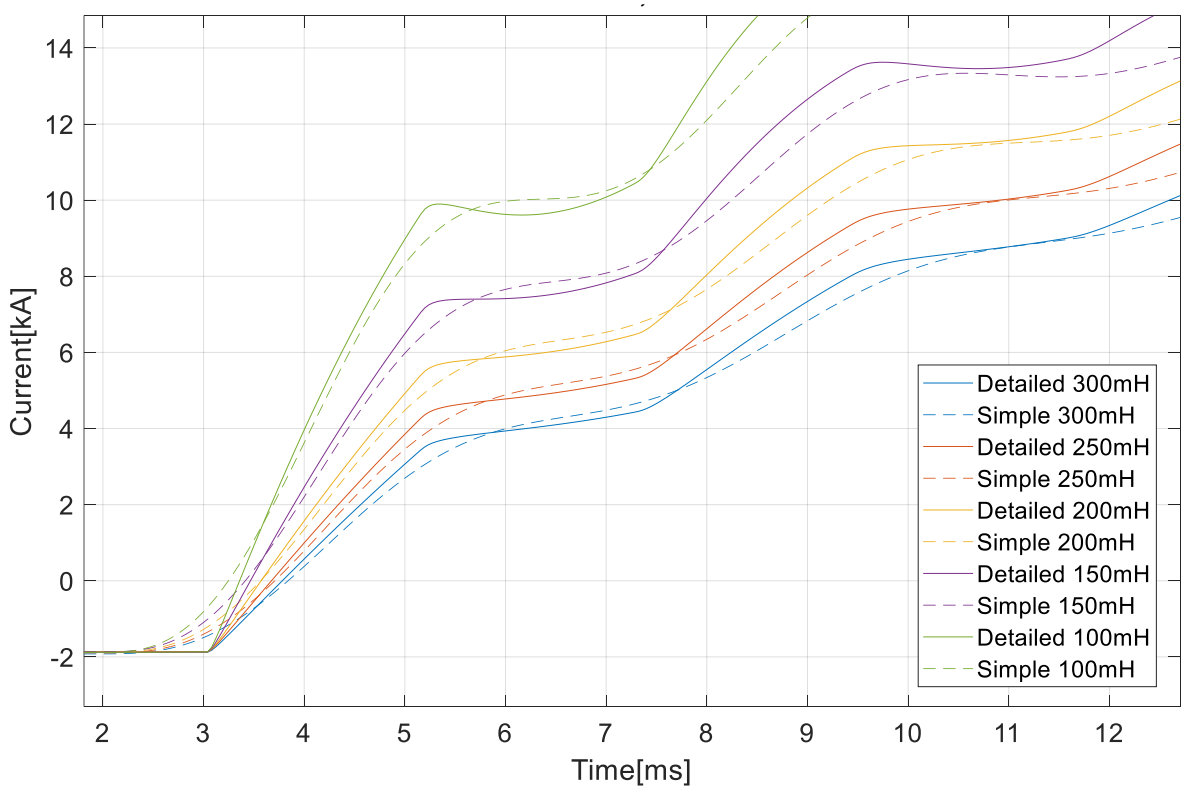


Figure 31 Test results for test scenario 2: detailed models (Averaged arm MMC model from use case in combination with cable wideband model) and simple models (AVM DC model in combination with cable pi-model)

5.4. Simplified model for traveling wave propagation

A cable fault provokes traveling waves propagating from the fault location to other parts of the grid. The initial voltage surge v_{init} at the fault location can be described as follows, where $v_{dc,0}$ is the pre-fault dc voltage, Z_c the characteristic impedance of the cable and R_f the fault resistance. Note that in the particular case of $R_f = 0\Omega$ the initial voltage surge is equal to the pre-fault DC voltage.

$$v_{init} = -v_{dc,0}\frac{Z_c}{Z_c + R_f}$$

The initial traveling wave is exposed to a damping factor d_q and distortion coefficient when propagating along the line. Neglecting the distortion, the amplitude of the propagating traveling wave at a distance d from the fault can be expressed as follows:

$$v(d) = v_{init}e^{-s\sqrt{LC}\,d}$$

At each intersection, parts of the traveling wave are reflected and transmitted according to the reflection coefficient $K_{1\to2}$ and transmission coefficient $T_{1\to2}$. The measurable voltage at the intersection is the transmitted traveling wave which is a superposition of the incident and reflected part. The transmission coefficient is equal to 2 for an open circuit ($Z_2 \to \infty$). Note that with an inductive termination the transmission coefficient gets close to 2.

$$K_{1\to2} = \frac{Z_2 - Z_1}{Z_2 + Z_1}, T_{1\to2} = \frac{2Z_2}{Z_2 + Z_1}$$

Hence, the measurable voltage at the cable termination is $v_T = v_{dc,0} + T\ v(d)$. In the case of DC reactors at the cable termination, the voltage can be of negative value with a maximum amplitude of v_{dc}. Considering this, the rise of fault current for a distant fault can be more significant than in case of a solid fault next to the DC reactor. In order to illustrate the described phenomenon, a test scenario according to Figure 32 is chosen. The cable is represented as frequency-dependent model. Two faults are compared:

- → Fault directly at the terminal (d=0km)
- → Fault at 100km from the terminal (d=100km)

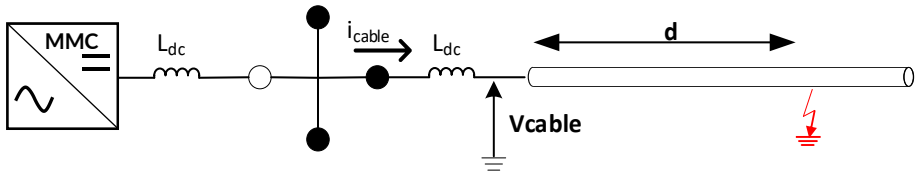


Figure 32 Test circuit for illustration of traveling wave propagation

Figure 33 compares the voltage and current evolution between the two fault cases. The pole-to-ground voltage is measured between cable end and DC inductor. It can be easily identified that the fault at 100km distance imposes a greater counter-voltage (-431kV) compared to a fault directly at the terminal (0kV). This leads to an initial voltage of 525kV+431kV=956kV across the DC reactor. The voltage is imposed for a time equal to two times the propagation time of the traveling wave ($T_{TW} = 2\,d/v_{TW} \approx 2\,100km/(\frac{185km}{ms}) \approx 1{,}08\text{ms}$). It should be noted that, in Figure 33, the fault inception time has been adjusted so that the two faults arrival are identical.

This allows to compare the fault current evolution. Due to the deeper voltage drop, a steeper rise of fault current can be identified for the distant fault case. With increasing simulation time, multiple voltage reversals can be identified, and the fault currents converge. However, for the first traveling waves, the difference can be significant and the fault inside the cable can be the dimensioning of the fault case.

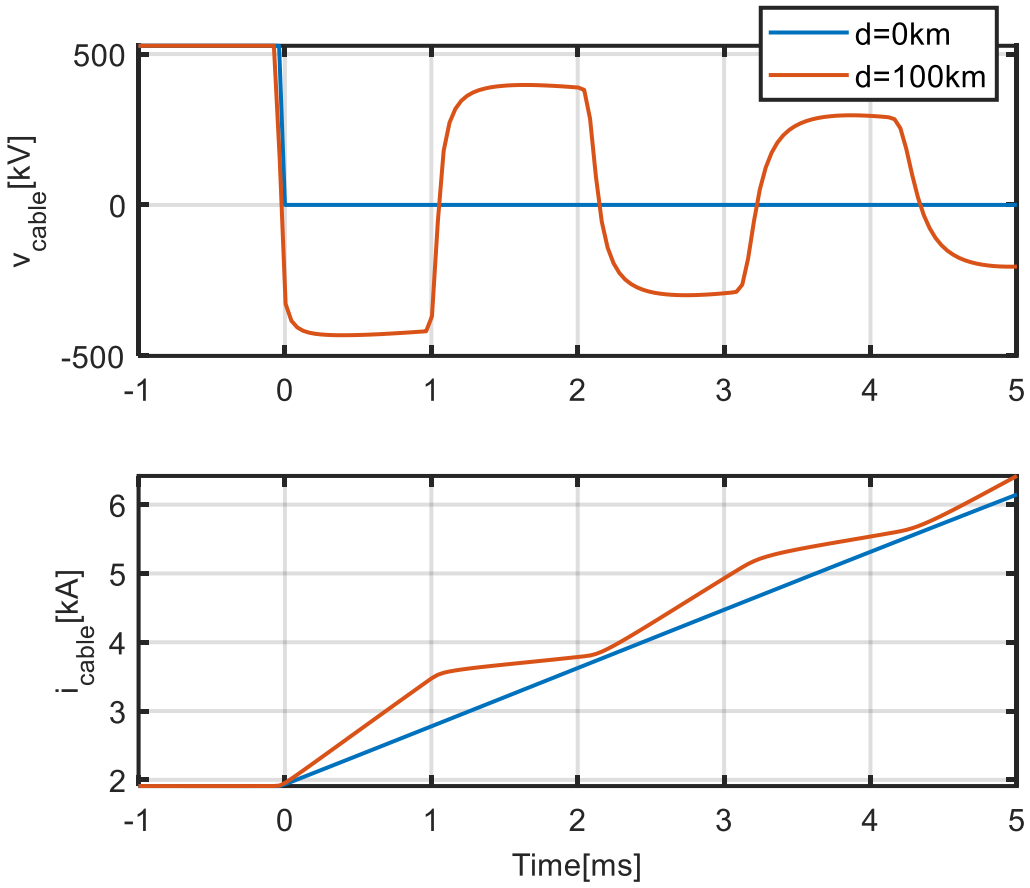


Figure 33 Voltage and current evolution for cable fault at 0km (blue) and 100km (red) from terminal

5.4.1. Model description

In the following, a simplified traveling wave generator will be introduced to consider cable faults with variable fault distance without needing to represent the cable as a frequency-dependent model. The model consists of a controlled voltage source connected to ground which replaces the frequency-dependent cable model represented in Figure 32. The imposed voltage (v_{TW}) is calculated in a separated circuit in the PSCAD environment. This circuit considers the traveling wave equations for the definition of damping coefficient, initial voltage surge as introduced above. It further assumes an idealized transmission coefficient equal to two.

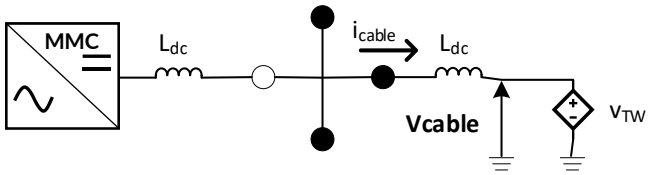


Figure 34 Traveling wave generator model

The model will allow to determine the dimensioning case of fault current evolution with variation of fault distance. The parameters as listed in Table 5 are used for the traveling wave generator model.

Table 5 Values for traveling wave generator model

Description	Parameter	Value
Characteristic cable impedance	Z_c	30Ω
Damping coefficient	d_q	0.18 1/s
Traveling wave speed	v_{wave}	185 km/ms

5.4.2. Model validation

To validate the traveling wave generator model, the fault current evolution and the voltage at the end of the cables are compared to the measurements during a fault on a cable using a frequency-dependent model (see Figure 35). The signal generator represents the voltage reversals in an accurate way in both amplitude and frequency considering the damping. The rise of fault current is also accurately represented for multiple traveling wave propagations.

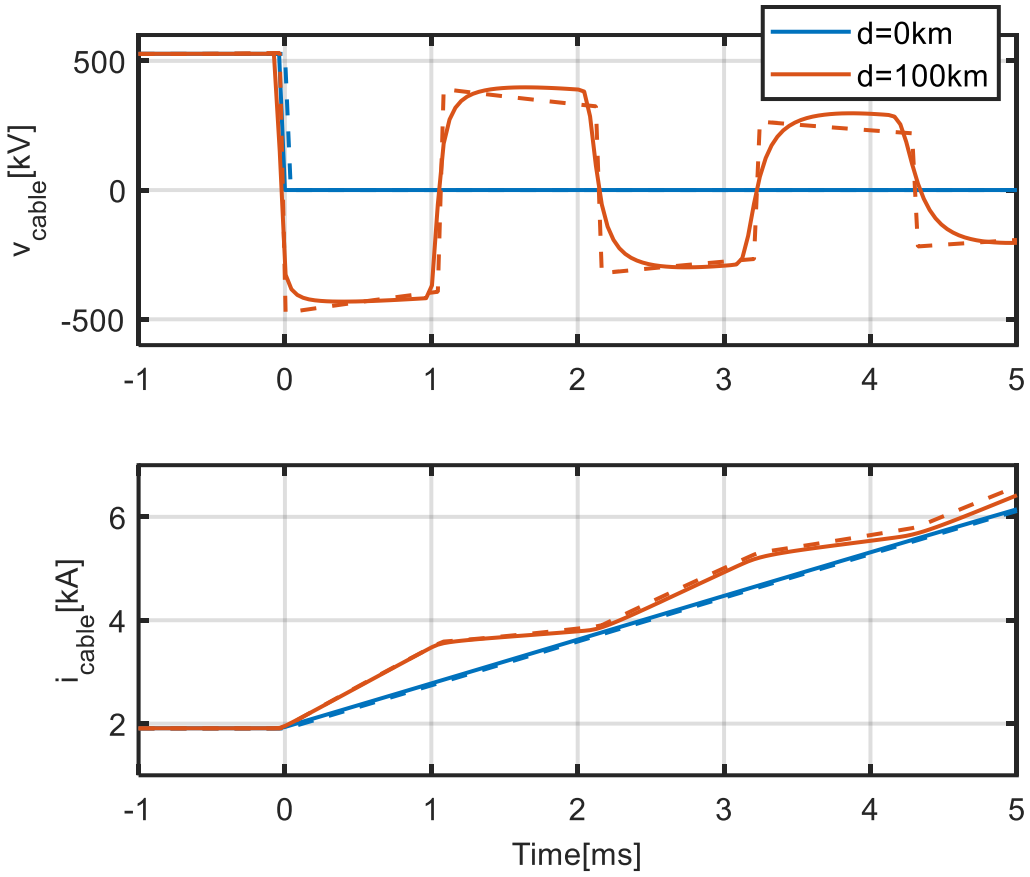


Figure 35 Validation of traveling wave generator model compared to frequency dependent cable model. Continuous line: frequency-dependent line model. Dashed line: travelling wave generator model.

5.5. DCCB model

Different approaches of DC fault current interruption have been proposed and successfully tested in the recent past [17]. In literature, DC Circuit Breakers (DCCB) are categorized in semiconductor based DCCBs, mechanical DCCBs (based on active current injection) and hybrid DCCBs (mechanical components in the main branch and semiconductors in the parallel branch [18]. The categorization is based on the current commutation principle from the main branch to the energy absorption branch. However, for all DCCBs, it accounts that a counter-voltage superior to the grid voltage needs to be generated to reduce the fault current. A generic non-vendor specific system model is used within this report, as shown in Figure 36 that can be described by the following equation:

$$v_{grid} = L_{grid}\frac{d}{dt}i_{grid} + R_{grid}\, i_{grid} + v_{SA}$$

It can be easily seen that the DC grid current i_{grid} decreases only if its derivative gets negative. This is the case if the condition of $v_{SA} > v_{grid}$ is fulfilled.

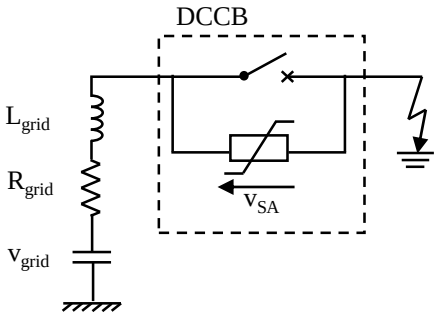


Figure 36 Simplified DC circuit

This leads to the conclusion that from a system perspective the decrease of the DC current and the dedicated energy absorption is mainly characterized by the counter-voltage across the DCCB, further denoted as "Transient Interruption Voltage (TIV)".

5.5.1. Model description

Considering this, the simplistic DCCB model that will be used in the STB consists of a simple controlled voltage source in series with a switch as shown in Figure 37. The voltage source is controlled according to the equation below, where T_{neut} is the fault neutralization time ($T_{neut} = T_{relay} + T_{op}$ and $T_{neut} = T_{relay} + 2T_{op} + T_{BFI}$ for primary protection and backup protection, respectively). The switch is opened at current zero T_{sup}.

$$v_{\mathrm{DCCB}} = \begin{cases} v_{\mathrm{TIV}}, & t \geq T_{\mathrm{neut}} \\ 0, & t < T_{\mathrm{neut}} \end{cases}$$

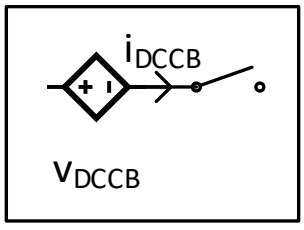


Figure 37 Simplistic DCCB model

The energy absorption of the arrester during the interruption process is calculated based on the following equation [16].

$$E_{\mathrm{DCCB}} = \int_{T_{\mathrm{neut}}}^{T_{\mathrm{sup}}} v_{\mathrm{DCCB}}\, i_{\mathrm{DCCB}}\, dt$$

5.5.2. Model validation

To validate the simplistic DCCB model, it is tested in a MTDC environment and more specifically in use case 1.1 with a fault at the offshore side of spoke 2. Figure 38 shows relevant DCCB quantities (top: fault current, middle: DCCB TIV, bottom: energy absorption during fault neutralization) for detailed models including non-linear surge arrester characteristics (solid) and simplistic models (dashed). Two simulation cases are shown: In blue color a DC reactor value of 180mH in combination with a DCCB operating time of 2ms and in orange color 720mH in combination with 10ms operating time. For both cases a relay time of 0.5ms is considered. Hence, the fault current interruption process starts at 2.5ms and 10.5ms respectively. The simplistic DCCB model imposes a constant TIV of 1.6pu which corresponds to the peak TIV of the surge arrester. With decreasing fault current, the surge arrester TIV slightly decreases due to the non-linear behavior which is not represented in the simplistic model. However, comparing fault current decrease and energy dissipation, the two models show very similar evolution. Hence, the simplistic DCCB model allows to estimate the SA energy rating and the fault neutralization time.

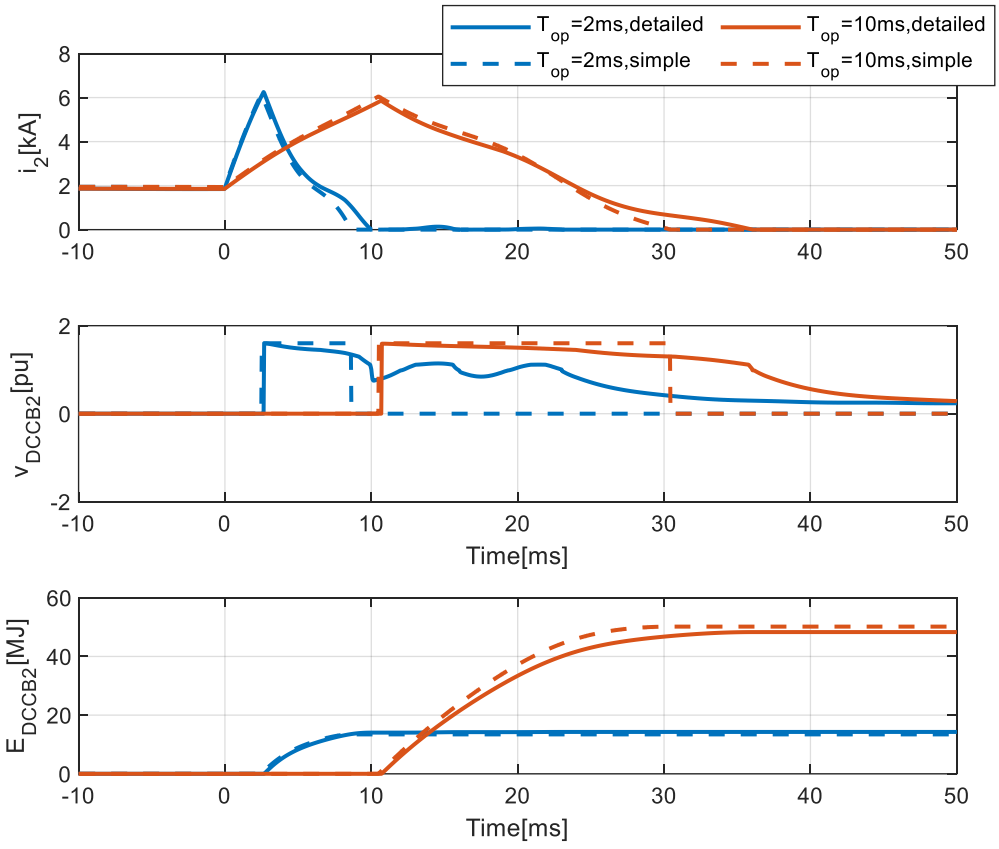


Figure 38 Validation of DCCB model for spoke fault in use case 1.1; Solid: Detailed use case models, dashed: Simplistic models for T_{op}=[2 10]ms, L_{dc}=[180 720mH]

5.6. Blocked MMC model for energization

In order to evaluate and compare different start-up sequences, a reduced MMC model in blocked state during energization is proposed. The main goal is hence to represent the capacitive charging phenomenon. A converter station can be charged either from the AC or from the DC side.

5.6.1. Energization from AC side

The current behavior during the energization process from the AC side is represented in Figure 39 taken from [19]. The current flows through 2 arms through the conducting diodes, charging only half of the capacitors. A simplified representation then consists of the 6 arms represented with equivalent submodule and diode, as presented in Figure 40.

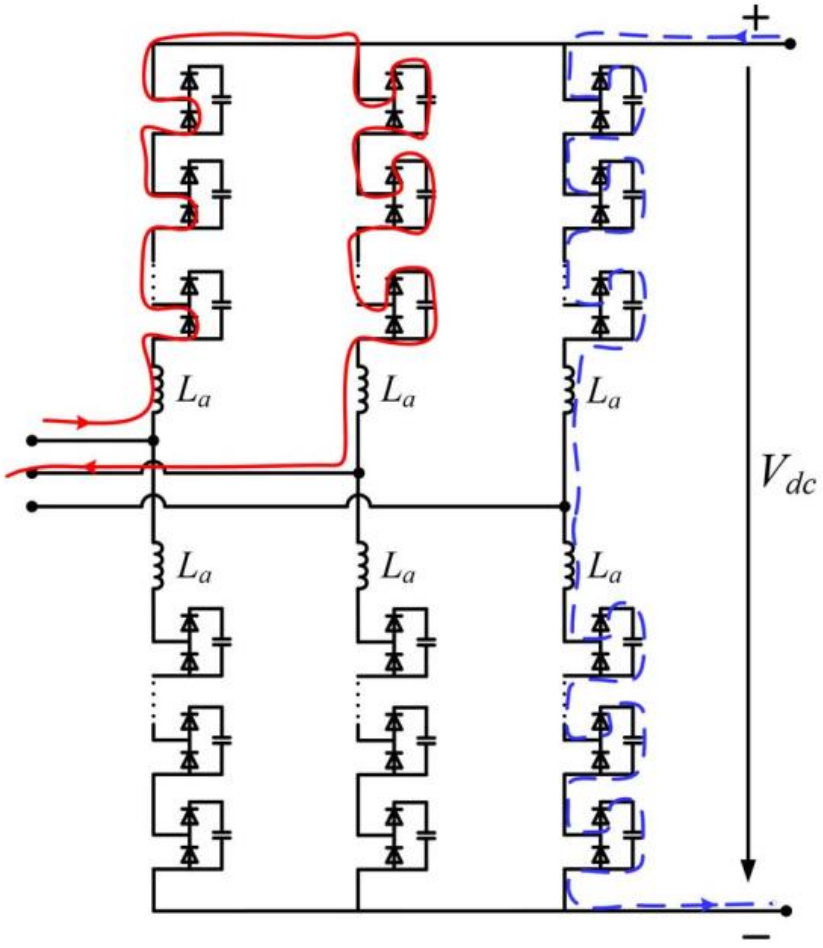


Figure 39: Current path during uncontrolled MMC energization from AC and DC sides, from [19]

The equivalent parameters are

- The arm inductance L_{arm}
- The arm capacitance $C_{arm} = \frac{C_{SM}}{N_{SM}}$
- The equivalent leg resistance $R_{leg} = 2R_{arm}$

Parameter	Symbol	Value
Arm inductance	L_{arm}	43 mH
Arm capacitor	C_{arm}	45.8 µF
Arm resistance	R_{arm}	1.34 Ω

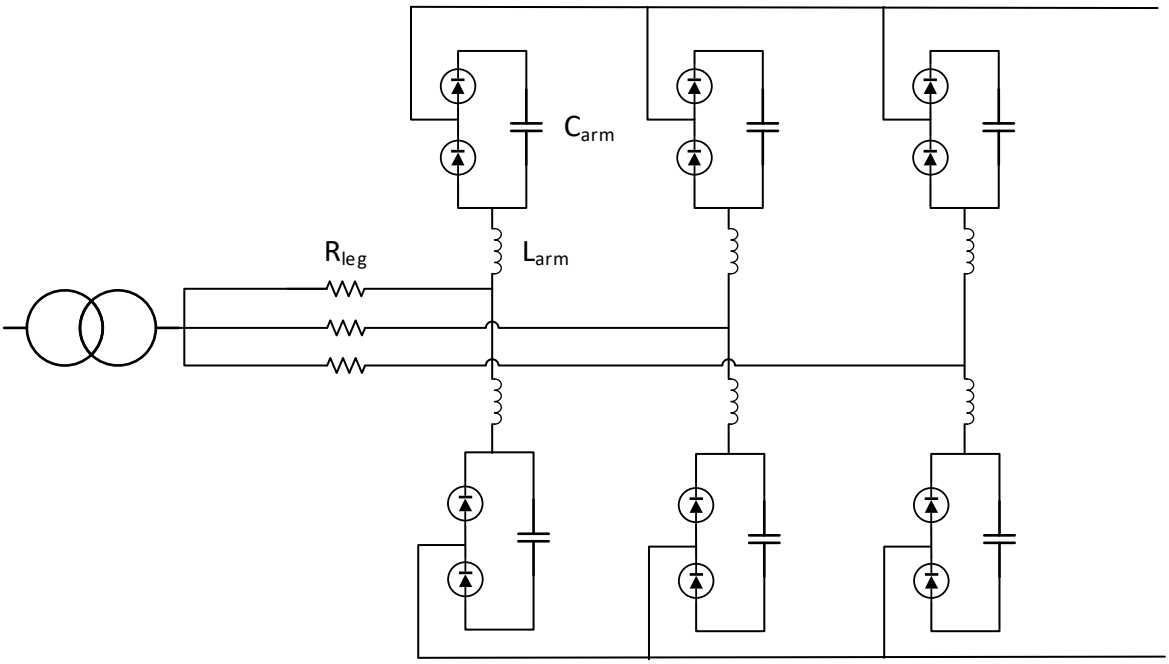


Figure 40: Blocked MMC model for energization from AC side

5.6.2. Energization from DC side

When energized from the DC side, assuming the AC side is open, the current flows through all the capacitors of one leg, the three legs being in parallel, as represented in Figure 39. An aggregated model can be used, with equivalent capacitor, inductance and resistance, as presented in Figure 41. An additional diode must be used to account for the current direction. The RLC equivalent parameters are $C_{eq} = 1.5C_{arm}$, $L_{eq} = \frac{2}{3}L_{arm}$, and $R_{eq} = \frac{2}{3}R_{arm}$.

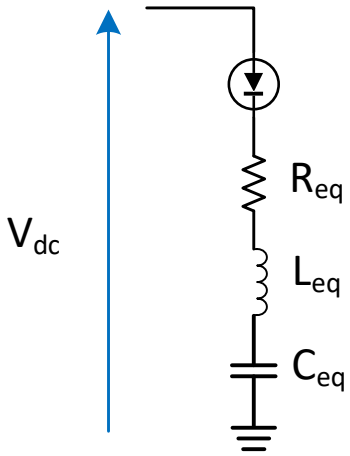


Figure 41: Blocked MMC model for energization from DC side

5.6.3. Model validation

In order to validate the proposed models for blocked MMC energization, the start-up sequence is decomposed into several steps where a single action is performed. The considered sequence for use case 1.1 is detailed in Table 6. To validate the blocked MMC model, all the components of the DC grid (onshore and offshore stations, cables) are first energized before the MMC are deblocked and the voltage is controlled. Only the first steps where the MMCs are not controlled are thus represented in the following figures. Pre-Insertion Resistors are associated with each switch, whose values are specified in Table 6. The AC side PIR was obtained from the input list, other PIR values are only initial value used for model validation and will be modified according to energization studies (see Section 8). Identical DCR values of 0.1H are used throughout the grid.

Table 6: Start-up sequence for step-by-step uncontrolled energization of MMC and cables

Time (s)	**Action**	**PIR value**
0.05	Onshore AC circuit breakers are closed, and onshore converters are energized	AC PIR = 25 Ohms
0.2	Onshore DC switches and offshore DCCB are closed and cables L1 and L2 are energized	Spoke PIR = 100 Ohms
0.5	Offshore converter switches are closed, and MMC1-2 and MMC2-2 are energized	Converter PIR = 500 Ohms
0.8	DCCB of interconnector are closed and L12 is energized.	Interconnector PIR = 200 Ohms

A simplified representation of the use case is implemented using the proposed blocked MMC models with energization from AC side for onshore stations and from DC side for offshore stations. The cables are represented using the introduced pi model. Finally, the AC side is represented similarly to the use case with a RL source and a transformer.

The comparison of the use case and the simplistic test benchmark is provided in Figure 42 for the onshore voltage, in Figure 43 for the interconnector voltage , and in Figure 44 for the onshore current. As the use case 1.1 is symmetric, only the quantities for the hub 2 (MMC2-1 and MMC2-2) are given, without any loss of generality.

The voltage and current during all the steps are perfectly represented by the STB. The energization of offshore MMC at t=0.5s causes a current spike which is limited by the large PIR (500 Ohms) placed at the MMC output switch. This PIR is inserted during 0.05s (after the closing of the switch). The bypass of the PIR reduces the resistance of the current path, causing a second current spike.

The overall behavior of the start-up is deemed sufficiently well represented with the simplified models to be evaluated through the STB. The deblocking of the MMC, which induces the energization of the remaining capacitor of the converter, is however not represented by the simplified model and requires further work.

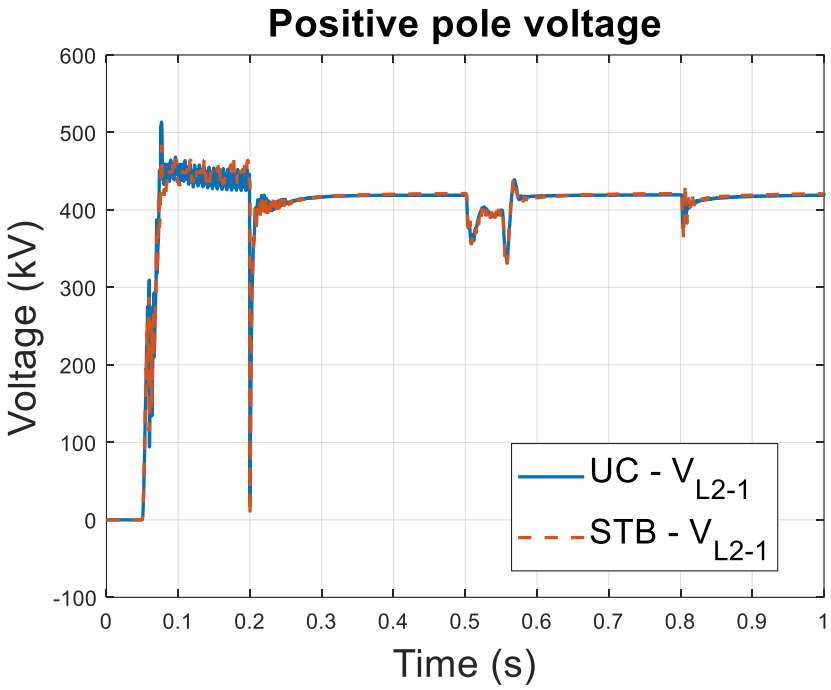


Figure 42: Comparison between STB and UC for positive pole voltage of MMC2-1 during uncontrolled energization of onshore MMC (t = 0.05s), spoke (t = 0.2s), offshore MMC (t = 0.5s), and interconnector (t = 0.8s)

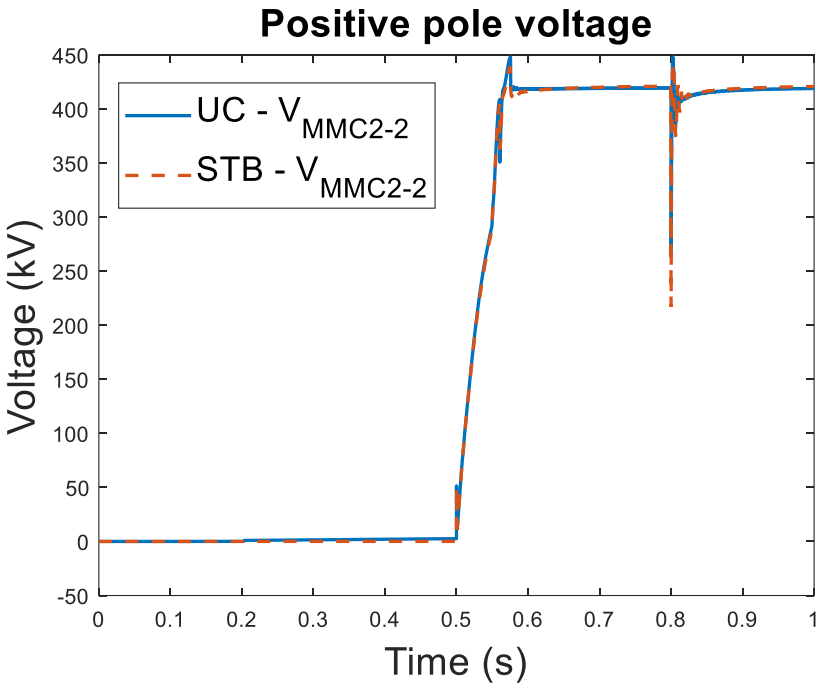


Figure 43: Comparison between STB and UC for positive pole voltage of L12 during uncontrolled its energization (t = 0.8s)

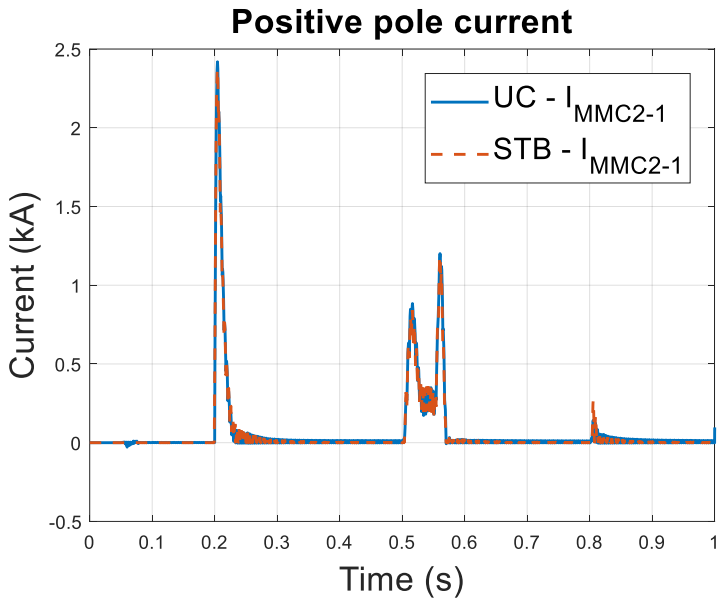


Figure 44: Comparison between STB and UC for positive pole current of MMC2-1 during uncontrolled energization of onshore MMC (t = 0.05s), spoke (t = 0.2s), offshore MMC (t = 0.5s), and interconnector (t = 0.8s)

6. Functional group - MTDC Grid Control

This section describes the methodology for specifying functional requirements related to the MTDC grid control and the relevant parameter ranges. Among the functional requirements and parameter ranges to be specified, certain aspects are inevitably dependent on the topology of a given system and cannot be generalized, and the so-called non-generic procedures are proposed. On the other hand, for other generalizable aspects generalized methodologies are proposed. To facilitate understanding, several sections are provided that illustrate empirical understanding.

6.1. Steady-state DC voltage range

In an MTDC grid under loaded condition, the voltage at each node differs due to resistive voltage drops in the transmission lines and cables. The steady-state DC voltage should be specified as the range within which all the performance requirement of the system apply without degradation of the performance quality. Although there are some ongoing initiatives by the international bodies for the standardization, no standardized value currently exists. This section describes the methodology for specifying the steady-state DC voltage range for the given use cases.

6.1.1. Methodology

The voltage drop that occurs in the system is essentially dependent on the configuration of the system. Therefore, it should be determined based on the planned system topology and the operating point. The longer the cables, the greater the voltage drop that occurs in the system. Therefore, if the system is planned to be expanded in the future, the steady-state DC voltage range should be specified taking that into account.

According to CIGRE TB563, the steady-state voltage range is considered as performance parameters, subject to study in the pre-specification phase. Steady-state power flow studies using simplified representation of the system would be suitable for this type of study.

As specified by the client, the maximum steady-state voltage of the cable is set at 525 kV, which is the rated voltage of the system. On the other hand, the minimum steady-state DC voltage level, which is the other bound of the steady-state voltage range, is still subject for specification. Therefore, specifying the steady-state DC voltage range consists of analyzing the maximum voltage drop in the grid while ensuring that this minimum voltage is not exceeded at any node in the steady state. To this end, the power flow conditions of the grid that yield the maximum voltage drop must be identified. This, too, is specific to the system.

For verification of the steady-state DC voltage range, we propose a simplified method using graph theory. This is based on the following characteristics of the DC system:

- Unlike AC systems, where the magnitudes of the voltages and their angles determine the power flow, in DC systems the power flow is determined solely by the voltages.
- Unlike AC systems, where the voltage can be increased by reactive power injection, in a DC system, power can only flow from higher to lower voltages.

From the above two points, it can be said that the maximum voltage difference in the grid occurs when the maximum current flows in the longest path in the grid. The proposed method is based on a simplistic representation of the DC grid by a graph, which is constructed using the following procedure to determine the validity of the steady-state voltage range.

1. Considering the grid as a graph (nodes: vertices, cables: edges (weight: length proportional to the resistance))
2. Finding the longest path between any two vertices in the graph using depth-first search

Note that a particular consideration for use case 1.2 and 2 is necessary in order to take into account the fact that certain AC/DC converters (MMC 4-1) and spoke cables (L4) have a power rating of 700 MW, not 1 GW. Since the voltage drop across the cable is proportional to the current, the corresponding maximum voltage drop in the cables rated other than 1GW are corrected by the appropriate factor α that multiplies the actual cable length (e.g. since L4 is rated at 700 MW, α=0.7).

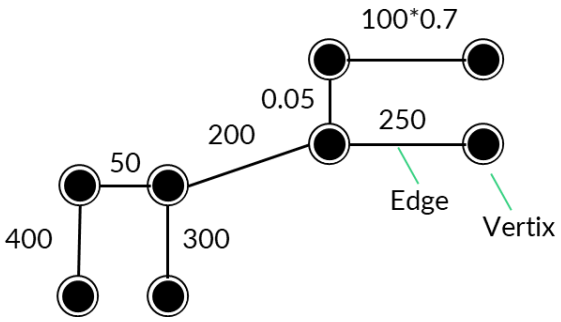


Figure 45 Example of graph representation (use case 1.2)

6.1.2. Results for use case 1.1

Although previously presented, the use case 1.1 is again illustrated in Figure 46. It is acknowledged that in this use case, the two onshore stations are connected to the same AC bus. Therefore, it is not practical to transmit power between the two onshore stations, namely MMC 1-1 and 2-1. Taking this particular feature into account, the longest feasible path between the two nodes is obviously 450 km, which is between MMC 1-2 and MMC 2-1. With the resistance value of the cable of 6 mΩ/km in steady state, the estimated voltage drop that can occur is 5.14kV, corresponding to 0.98%.

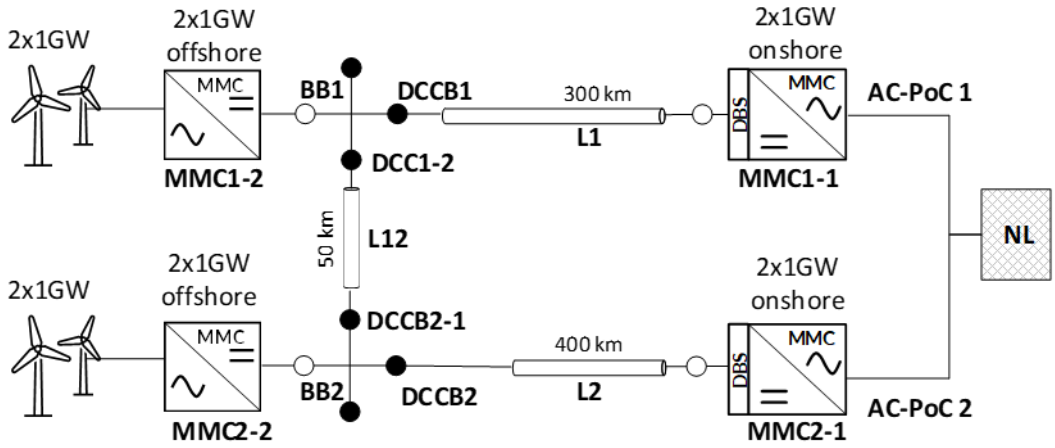


Figure 46 Overview of the subject system: Use case 1.1

For the validation purpose, the identified worst-case scenario is tested on the PSCAD simulation using the models validated in 5.2.1.2. The voltage of the injection point should be set as the maximum voltage of 525 kV. The identified worst-case scenario corresponds to the case of a maximum power transmit from offshore station

MMC 1-2 to the onshore station MMC 2-1, with zero power injection from MMC 1-1 and MMC 2-2. The obtained voltage and power profiles are summarized in Table 7 . As seen, a voltage drop of 5.0 kV, approximately 0.6%, can occur in the grid. Although small in value, this can still have a noticeable effect depending on the DC voltage droop gain because the DC voltage droop action takes effect on the deviation measurement value from the voltage set-point value (See 0 for more details). Therefore, unreasonably small droop gain settings may result in large power deviations even for such a small steady-state voltage drops.

Table 7 Worst-case steady-state power flow condition for use case 1.1

	Steady-state operating point	
	AC active power [MW]	DC voltage [kV]
MMC 1-1	0	525.0
MMC 1-2	1000	525.0
MMC 2-1	-964.8	520.0
MMC 2-2	0	524.4

In practice, the switching of MMC sub-modules will result in the voltage harmonics whereby the DC voltage oscillates around its average steady-state value at the switching frequency. Therefore, the steady-state voltage range should be defined taking into additional margin for them.

6.1.3. Results for use cases 1.2

The proposed identification method of the longest path and the estimation of the maximum voltage drop using the graph theory has been applied to use case 1.2. In Figure 47, the topology of use case 1.2 is recalled. The longest distance between any two nodes in use case 1.2 was identified as the path between MMC 2-1 and MMC 3-1, corresponding to 900 km in total. The estimated voltage drop is 10.29 kV (1.96%). Similar to the study on use case 1.1, the estimated DC voltage drop is validated by simulations. The identified worst-case scenario corresponds to the case of a maximum power transmit from onshore station MMC 2-1 to MMC 3-1, or vice versa. The obtained voltage and power profiles summarized in Table 8 show that a voltage drop of 10.2 kV occurs, which is in good agreement with the estimated value.

It is important to note that, unlike use case 1.1, the stations other than the two associated with the longest path can take any operating point as long as the rated current is flowing in this path. In other words, even if power is exchanged between other stations (e.g. between MMC 1-2 and MMC 1-1), as long as the rated current is flowing in this path, all the voltages at the nodes in the system will fall within this range.

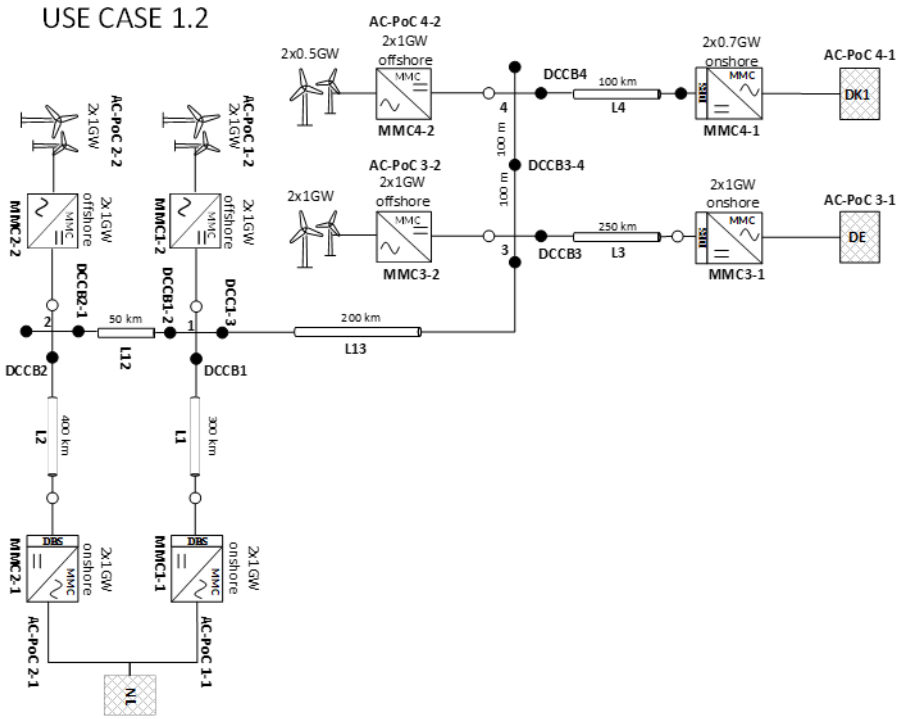


Figure 47 Overview of the subject system: use case 1.2

Table 8 Worst case steady-state power flow condition for use case 1.2

	Steady-state operating point	
	AC active power [MW]	DC voltage [kV]
MMC 1-1	0	519.9
MMC 1-2	0	519.9
MMC 2-1	+1000	525.0
MMC 2-2	0	520.5
MMC 3-1	-955	514.8
MMC 3-2	0	517.7
MMC 4-1	0	517.7
MMC 4-2	0	517.7

6.1.4. Results for use cases 2

Figure 48 recalls the topology of use case 2. In general, a meshed grid tends to have a smaller impedance between the nodes, so the voltage drop that occurs within the grid is smaller than that of a radial grid, e.g., use case 1.2. However, it is deemed important to consider the case where the grid becomes radial due to faults or maintenance. Therefore, the same algorithm was applied for each interconnecting cable being out of service case, and the possible maximum voltage drop values were estimated for each case. The obtained results are summarized in Table 9. As can be seen from these results, the maximum voltage drop of 12.6 kV, roughly 2.4 %, is estimated in case of L13 being out of service. The results imply that even though the voltage drop is generally reduced by the meshed grid in normal operation, a larger voltage drop may occur when some cable is out of service.

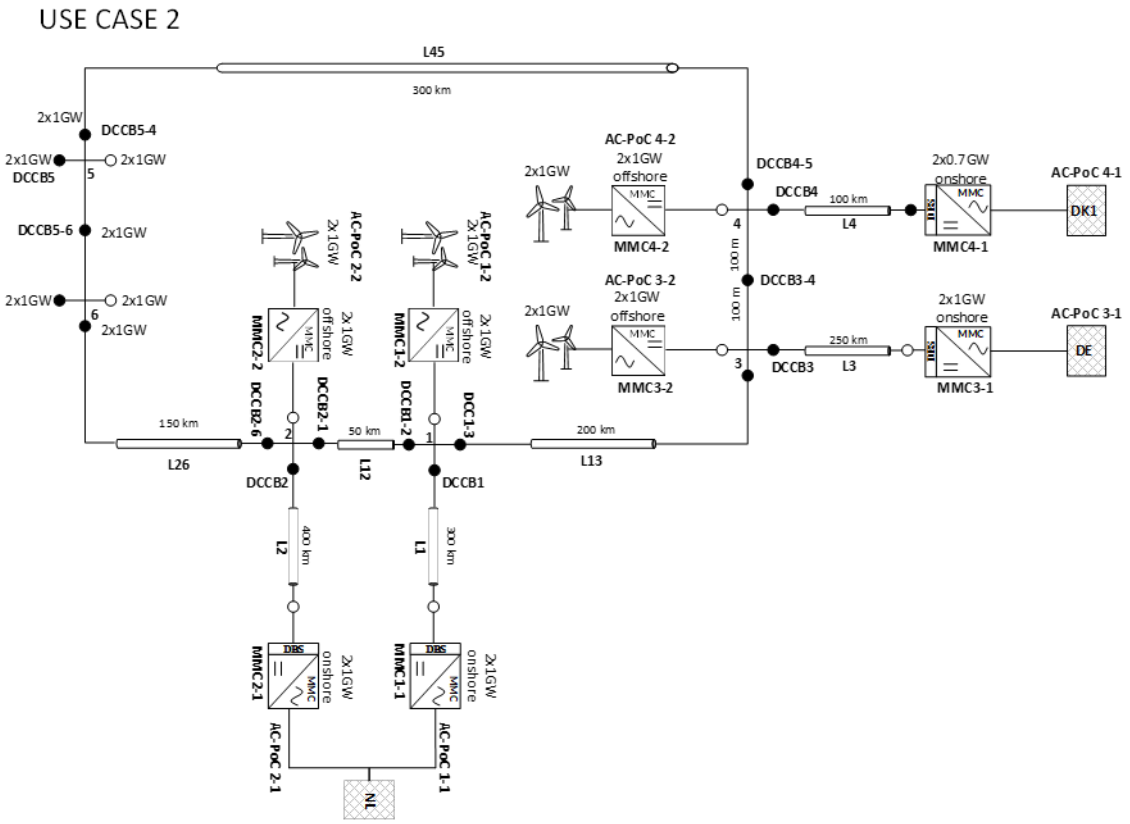


Figure 48 Overview of the subject system: use case 2

Table 9 Estimated maximum DC voltage drop in case of loss/maintenance of the lines in use case 2.

Case of loss/maintenance of line	Length_max	kV	pu
L12	1050*1	12.0	0.023
L13	**1100**	**12.6**	**0.024**
L34	1020*2	11.7	0.022
L45	900	10.3	0.020
L26	950	10.9	0.021

*1As in use case 1.1, the maximum power exchange between the two was excluded, given that MMC 1-1 and MMC 1-2 are connected to the same AC bus.

*2L4 is rated at 700 MW, and hence corrected by the factor of 0.7 and considered as an equivalent 70km cable here.

6.1.5. Summary of studies on use cases

The maximum voltage drop that occurs within the DC grid can be approximately estimated by the rated current flowing between the two nodes with the longest distance. As confirmed by the simulation results, the proposed method can estimate the maximum voltage drop that can occur in the system relatively easily.

Table 10 and Figure 49 summarizes the obtained results for use cases 1.1, 1.2 and 2. The results obtained suggest that specifying a narrower steady-state voltage range may impose a constraint on future system expansion. In AC systems, there is a stability limit determined by voltage stability, and if this limit is exceeded, voltage collapse may occur, so the steady-state operating voltage range must be strictly specified. However, there is no such stability limit for DC systems. Therefore, the specification of the steady-state range should have a sufficient margin in anticipation of future system extension.

Table 10 Summary of the possible maximum voltage drops in use cases.

Use case	Longest distance	Estimated maximum voltage drop	Upper level of the normal DC pole operating voltage range (UDC_{pole_max})	Lower level of the normal DC pole operating voltage range (UDC_{pole_min})
Use case 1.1	450 km	5.14 kV (0.98 %)	525	520.0 kV
Use case 1.2	900 km	10.3 kV (2.0 %)		514.8 kV
Use case 2 (in case of loss/maintenance of line)	1100 km	12.6 kV (2.4 %)		512.4 kV

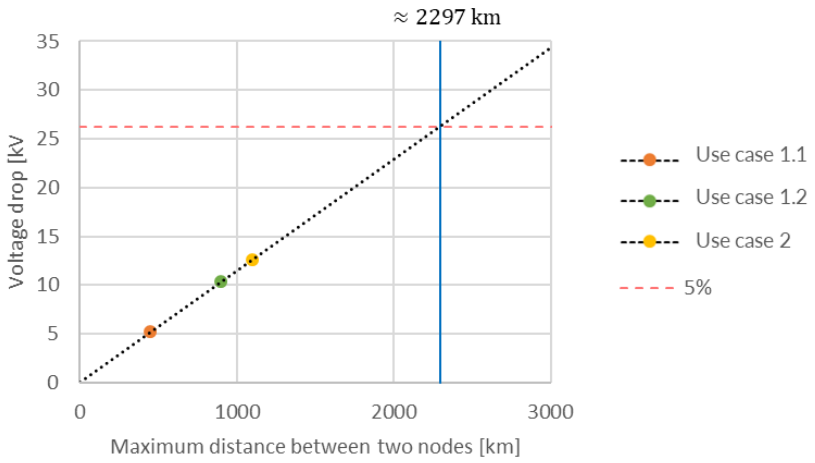


Figure 49 Correlation between distance and maximum voltage drop.

Another important point to consider is the difference in implication between the pole-to-ground voltage and the pole-to-neutral voltage, which is conceptually illustrated in Figure 50. While the minimum "pole-to-ground voltage" for normal operation, UDC_{pole_min}, is an important parameter to be specified for the equipment design according to the CENELEC, the operational limit of the converter station, such as active power and reactive power transfer capability, is influenced largely by the minimum "pole-to-neutral voltage". Considering a bipolar system, in ideal operating condition where the currents in the positive and negative poles are balanced, the pole-to-ground and pole-to-neutral voltage can be nearly identical. However, when the positive and negative poles are unbalanced, a voltage drop of twice the ideal case can occur in the pole to neutral voltage in the worst case. Particularly for the onshore stations, the converters and the tap changers of the AC transformers shall be designed in order to guarantee that the desired active and reactive power transfer capability can be achieved considering the minimum pole-to-neutral voltage.

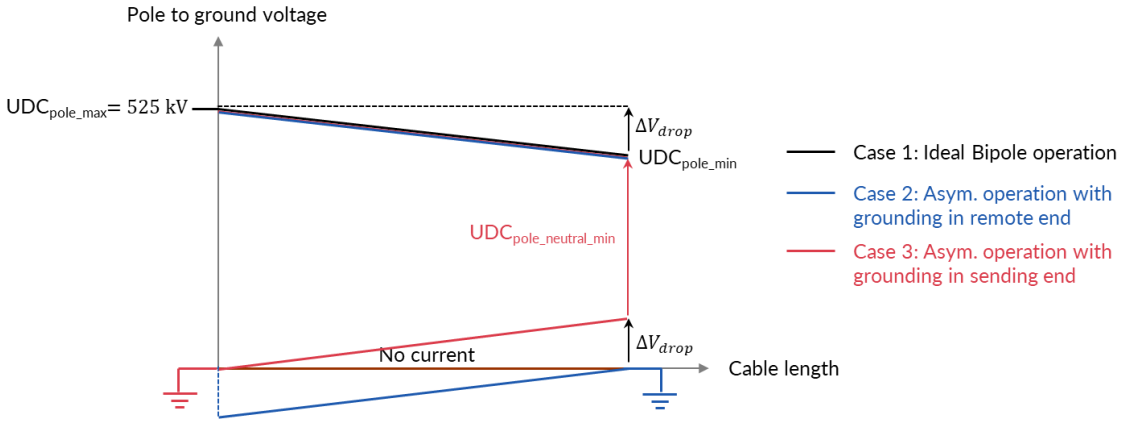


Figure 50 Difference in implication between Pole-to-ground voltage and Pole-to-Neutral voltage

6.1.6. Reduced DC grid voltage operation

The customer raised the special need that, in order to ensure the insulation of degraded cable, the MTDC grid should be capable to operate at a reduced DC voltage. Operation at voltages significantly lower than the rated voltage inevitably requires compromises and reduction of the PQ capability during the reduced DC voltage operation. It was agreed that the extent to which a reduction in operating capacity is acceptable is left to the operator's decision. However, it should be noted that there are operating limits for HB-MMC determined by the well-known modulation index

$$M = \frac{\sqrt{2}V_{acLLrms}}{\sqrt{3}\frac{U_{dc}}{2}} < 1$$

It is known that by injection of third harmonics, this limitation of the modulation index can be relaxed from 1 to $2/\sqrt{3}$ [20].

Considering the rated voltage of the valves on the AC side of the onshore stations, $V_{acLLrms}^{Max} = 300$ kV, the theoretical allowable steady-state minimum DC voltage requirement U_{dc}^{Min} is given as

$$\sqrt{2}V_{acLLrms}^{Max} < U_{dc}^{Min} = 424.3\ \text{kV} = 0.81\ \text{p.u.}$$

The implication of this value is that if the DC voltage is greater than about 0.8 p.u., then the rated AC voltage can be synthesized without causing overmodulation. However, the required AC voltage amplitude depends on the operating point of the power supply. Since the generation of reactive power requires a converter output voltage higher than the amplitude of the AC grid, this limitation in the modulation index imposes stringent capacitive power capability. The use of a tap changer in the interface transformer mitigates this limitation imposed by the modulation index in steady-state operation and allows the converter to make full use of its capabilities.

The theoretical limitation on the DC voltage imposed by the modulation index varies as the amplitude of the AC grid voltage changes. Considering the case of 1.10 p.u. of the valve side AC voltage of the onshore stations, i.e., $V_{acLLrms}^{Max} = 330$ kV, the theoretical limit of the DC voltage requirement given by the modulation index increases thus to

$$\sqrt{2}V_{acLLrms}^{Max} < U_{dc}^{Min} = 466.7\ \text{kV} = 0.89\ \text{p.u.}$$

In practice, however, reactive power provision is unlikely to be required when the AC grid voltage is already higher than the nominal value. Importantly, when specifying the required active and reactive power capability, the needed AC and DC voltage levels must be clearly stated.

6.1.7. FR and PR definition

Table 11 Functional requirements related to steady-state DC voltage range

ID	**Functional requirement**
General 3	The steady-state DC voltage range should be defined such that all target operating points can be covered.
General78	The AC/DC converter should be capable to operate at a reduced DC voltage. During the reduced DC voltage operation, the PQ power capability at the corresponding DC voltage level should be satisfied.

Table 12 Parameters related to steady-state DC voltage range

ID	Symbol	Characteristic/Events	Range	Comments
4	UDCpole_max	upper level of the normal DC pole operating voltage range	525 kV (or 1 p.u.)	
3	UDCpole_min	lower level of the normal DC pole operating voltage range	$[499 - 512]$ kV (or $[0.95 - 0.975]$ p.u.)	Lower bound set to 5%
133	UDCpole_min_reduced	lower level of the normal DC pole operating voltage range in reduced DC voltage operation"	$[424.3 - 499]$ kV (or $[0.81 - 0.95]$ p.u.)	This value should be considered in specifying the PQ capability in reduced DC voltage operation

6.2. Fixed DC voltage control mode

The fixed DC voltage control is an extension of the traditional master/slave control method in conventional point-to-point systems, where only one station in the system is responsible for maintaining the DC voltages of the system constant while the other stations follow active power set-points. In the following, the specifications related to this control are discussed separately for the requirements for the AC/DC converter in this control mode and the requirements for the controlled DC voltage of the system.

6.2.1. Specification of the DC voltage controller

The characteristics of the DC voltage controller itself are determined by the assigned control parameters. Since the control parameters are usually defined in a per-unit basis, the effective performance depends on the rating of the converter and other factors. Furthermore, it cannot be easily verified externally by observing the curves of the DC voltage. Therefore, they must be specified in the verification procedure in the specified configuration.

The discussion below is based on the PI controller, which is commonly used for fixed DC voltage control. A PI controller is characterized by only two parameters, namely, the proportional and integral gains: K_p and K_i. K_p and K_i do not independently determine the controller performance, nor are they in an externally verifiable form. Therefore, we introduce response time T_r, which is externally verifiable, and consider it as the subject of parameter range to be specified. The response time of the fixed DC controller is defined here as the time to reach the band of ±5 % in case of a step reference change.

The tuning of this controller is based on the assumption that the response time of the internal control loop is sufficiently faster than the desired response time of this controller; hence, the inner loop dynamics is neglected. Then, it is known that the general behavior of the MMC under the fixed DC voltage control can be represented by the block diagram shown in Figure 51

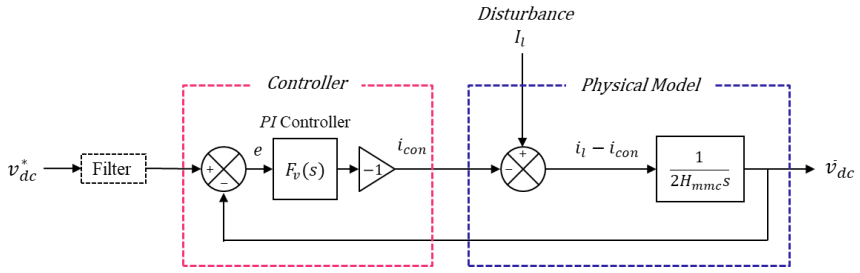


Figure 51 Simplified model of the MMC under the fixed DC voltage control mode [21]

whose closed-loop transfer function of the DC voltage control is given by

$$\frac{v_{dc}}{v_{dc}^*} = \frac{1 + \frac{K_p^v}{K_i^v}s}{\frac{2H_{mmc}}{K_i^v}s^2 + \frac{K_p^v}{K_i^v}s + 1}.$$

This is compared with the characteristic second-order transfer function, whose dynamics is known as

$$TF(s) = 1 + \frac{2\zeta}{\omega_n}s + \frac{1}{\omega_n^2}s^2$$

where ζ is the damping ratio and ω_n is the natural frequency.

Then the two controller gains can be expressed as the function of the desired response speed T_r as follows:

$$K_p^v = 4\zeta\omega_n H_{mmc}$$
$$K_i^v = \frac{1}{T_i^v} = 2\omega_n^2 H_{mmc},$$

where H_{mmc} is the electrostatic constant of the MMC reflecting the equivalent size of the capacitor, and given by

$$H_{mmc} = \frac{1}{2}\frac{C_{eq} v_{dc,n}^2}{S_b}$$

where $v_{dc,n}$ is the nominal DC voltage and the S_b is the rated apparent power.

Then, for $\zeta = 0.7$, the response time T_r is related to ω_n by

$$T_r \approx \frac{3}{\omega_n}$$

The validity of the tuning method introduced above, and the proposed controller verification procedure of the controller are demonstrated in the following.

The verification of the DC voltage controller itself should be done separately from the system. Figure 52 depicts the proposed setup for the verification setup. The converter model is interfaced with a simple current/power source on the DC side connection point. Then, the step change in the DC voltage controller reference v_{dc}^* is generated (e.g., $v_{dc}^* = +5\%$). The voltage should be measured at the PoC-DC. The proposed set-up for the verification procedure was implemented in PSCAD using the previously validated AVM AC/DC model of the MMC. Then, the step response was observed for different values of the desired T_r. The obtained results are shown in Figure 53, where the dashed lines indicate the $\pm 5\%$ band around the new reference value. As can be seen, the measured DC voltage reaches the 5% band within the specified T_r value.

In summary, the response time is an adequate parameter to specify the dynamic behavior requirements in an externally verifiable manner in place of the K_p and K_i values. Then, the appropriate range of values for this T_r is specified from the system's point of view.

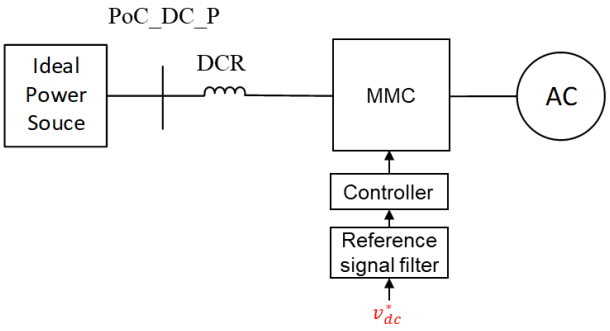


Figure 52 Proposed verification setup for the fixed DC voltage controller

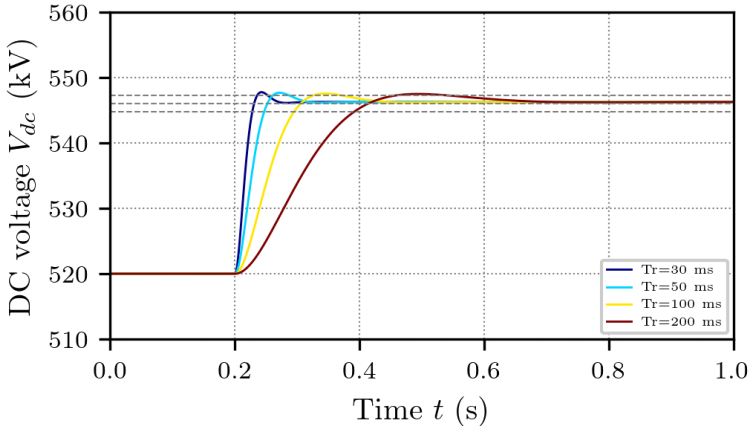


Figure 53 DC voltage step response with different response time

6.2.2. System requirements for dynamic over- & under voltage containment

In conventional HVDC PtoP systems, the tuning of the DC voltage controller, and thus the selection of response time, is done in terms of dynamic overvoltage and undervoltage containment. It is known that the behavior of a typical cable-based HVDC system where no DCR is installed can be well represented by the simple block diagram, where the equivalent total capacitance of the DC grid is represented by its electrostatic constant H_{total}, as shown in Figure 54 [21].

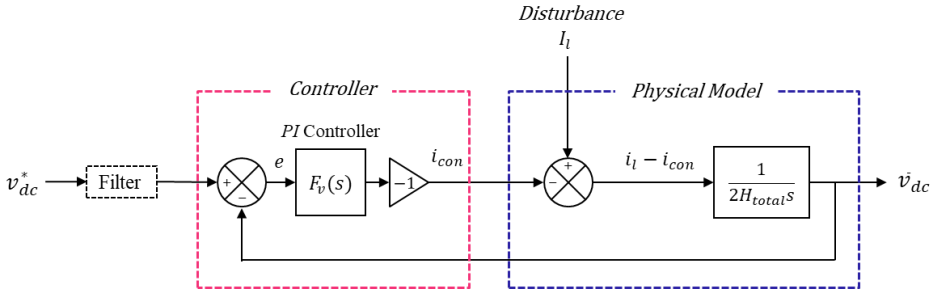


Figure 54 Simplified closed-loop model of typical HVDC system under fixed DC voltage control

The transfer function from the disturbance I_l to the error in DC voltage, $e = v_{dc}^* - v_{dc}$, is derived as:

$$TF(s) = \frac{\frac{1}{2H_{total}s}}{1 + F_v(s)\frac{1}{2H_{total}s}}$$

where $F_v(s) = K_p + K_i/s$, and H_{total} is the total electrostatic constant of the DC grid. Considering the worst scenario with a step change of the current corresponding to 1 GW, i.e., $I_l = I_{dis} = P_{dis}/V_{dc,nom}$, the response of the error signal in time domain is given by

$$e(t) = L^{-1}\left\{TF(s) * \frac{I_{dis}}{s}\right\} = \frac{I_{dis}}{2H_{total}\omega_n} e^{-\zeta\omega_n t} \sin\left(\omega_n\sqrt{1-\zeta^2}t\right)$$

where

$$\omega_n = \frac{3}{T_r}\sqrt{\frac{H_{mmc}}{H_{total}}}, \qquad \zeta = 0.7\sqrt{\frac{H_{mmc}}{H_{total}}}$$

The time when the error reaches its peak can be calculated by setting the time derivative of $e(t)$ equals to zero, i.e. $\frac{de(t_{peak})}{dt} = 0$, and given by

$$t_{peak} = \frac{\tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}}{\omega_n\sqrt{1-\zeta^2}}$$

Then, substituting t_{peak} into $e(t)$ yields the peak value of the error

$$e_{peak} = e(t_{peak}) = \frac{I_{dis}}{2H_{total}\omega_n} e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}}$$

Finally, denoting the pre-contingency DC volage by $V_{dc,0}$, the peak DC voltage value can be given by

$$V_{peak} = V_{dc,0} + e_{peak}.$$

The validity of the derived expressions is confirmed by a simulation of detailed use case 1.1. MMC 1-1 is set to the fixed DC voltage control mode. The induced scenario is a sudden blocking of the offshore AC/DC converter station MMC 1-2 at t=0.5s, resulting in a loss of 500MW injection. No DCR is considered, and T_r is set to 100 ms.

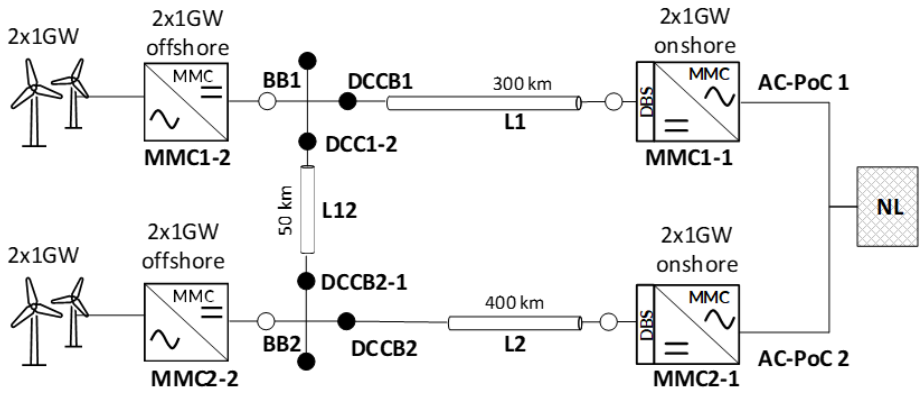


Figure 55 Example case for the demonstration (use case 1.1)

The peak time and the peak voltage were estimated as 79ms and 483.7 kV, respectively. In Figure 56, the simulation results and estimated peak timing and voltage are plotted. It can be seen that the peak timing and the peak value are estimated accurately.

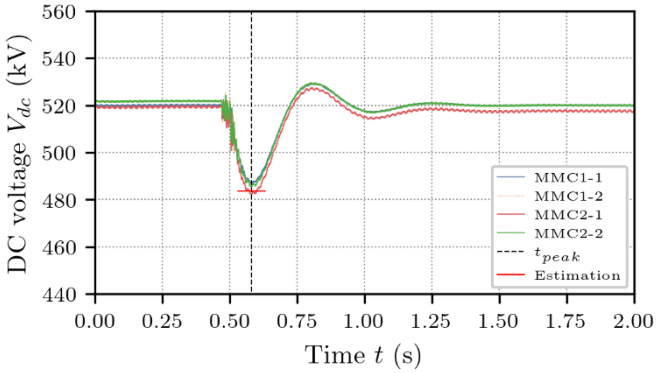


Figure 56 Validation of expressions.

The derived equation gives the peak value of the voltage at the specified value of T_r for any given system capacitance and disturbance magnitude. The peak value of the voltage increases as the system capacitors decrease. Assuming a 1 GW disturbance to the two-terminal DC grid, which is the minimum operable system configuration, the peak DC voltage and the peak timing with respect to the value of value of T_r are plotted in Figure 57. As seen, the voltage variation is approximately 0.2 pu for $T_r = 120$ ms. Therefore, it is theoretically recommended a value of T_r lower than 100 ms in order to contain the dynamic over- and undervoltage within 20%.

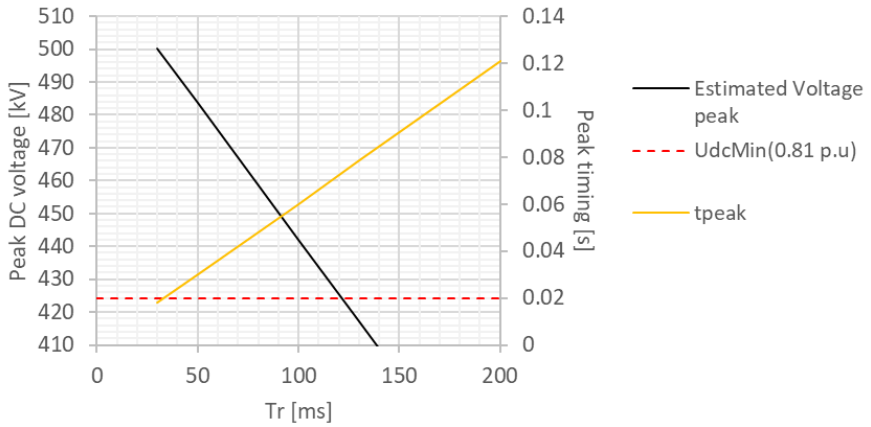


Figure 57 Peak DC voltage value and timing for different Tr.

One of the important parameters that determines the behavior of the DC voltage is the MMC energy level which determines the electrostatic constant of the MMC, Hmmc. To investigate this effect, the value of Hmmc was varied from 20, 40, and 100 ms, and the results were plotted. Figure 58 shows the results. As observed, for the same value of Tr, the peak DC voltage value decreases significantly as the value of Hmmc becomes smaller. This is because a smaller capacitor causes a larger voltage change for the same current change. Therefore, when designing the MMC with small values of Hmmc, a correspondingly faster DC voltage control is required.

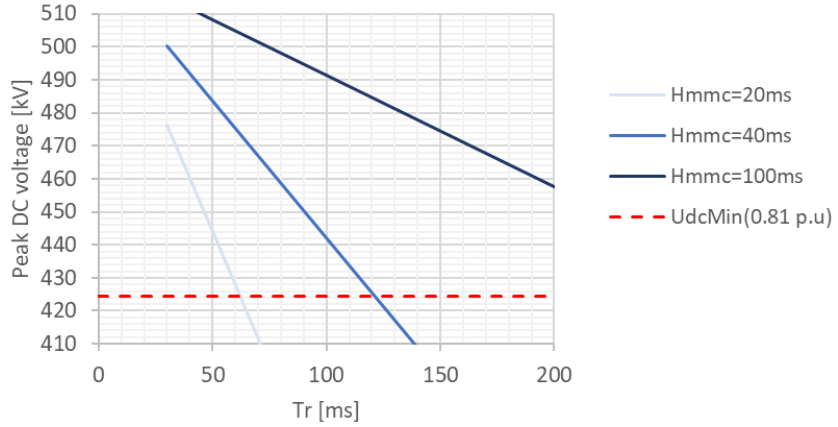


Figure 58 Sensitivity analysis of the Peak DC voltage value for different values of Hmmc.

The conclusion here was based on the strong assumption that no DCRs are present in the system, and thus a relatively simple analytical expression allowed to reproduce the dynamic characteristics of the system. However, this is not the case when there are many DCRs in the system, since each DCR adds a state to the system, and they can significantly affect the overall system characteristics depending on their values. Therefore, even if the conclusions here provide a guideline for the specification of fixed DC voltage controllers, the effect of the DCR size on the system under the fixed DC voltage control mode needs to be further elucidated by complementary studies on the stability in the following section.

6.2.3. System requirements for stability

The system behavior varies greatly depending on the system topology, the DCR size, etc., even for the same control parameters. The following is an illustrative example of how the system's response to a disturbance may vary with these parameters. The simulations were carried out using the detailed use case 1.1. For two different combinations of DCR size and T_r value, the dynamic responses of the system in case of the blocking of MMC 1-2 were observed.

The obtained results are shown in Figure 60. The voltages were measured at the busbar, i.e. behind the DCR seen from the MMC. The two combinations clearly show different behavior. The difference between the two shows that the size of T_r and DCR has a significant effect on the damping of the system. Therefore, in the following, using the developed STB validated in section 5.2.1.2, the acceptable combination of the DCR size and the DC voltage controller response time T_r that ensures the system stability will be determined.

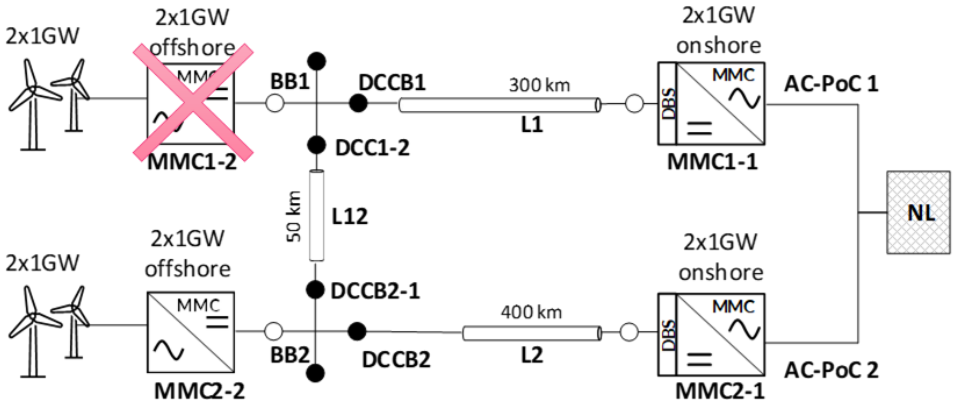


Figure 59 Example case for the demonstration (Use case 1.1)

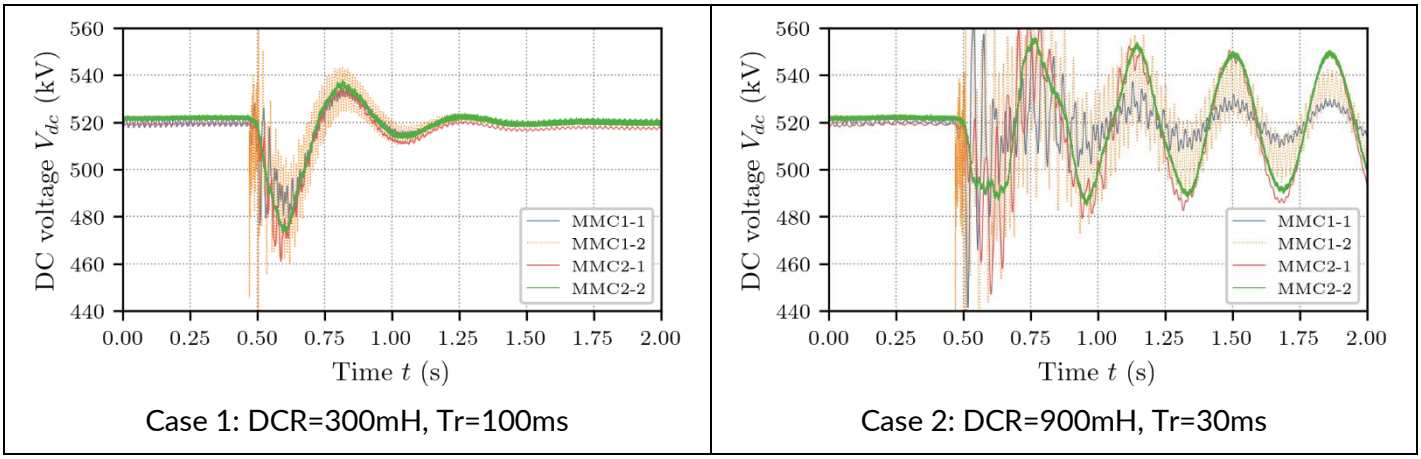


Figure 60 Simulation results of use case 1.1 : DC voltages measured at PoC-DCs in case of blocking of MMC 2-1 with two different combinations of the DCR size and Tr (values in two combinations are indicated below each figure)

In order to estimate the damping of the system, the system must be excited. As seen in the DC voltage measurements demonstrated above, the blocking of a converter generates significant noises that make it difficult to process numerically. For that reason, the system is excited by a step change of the voltage set-point. The focus is given to the common DC voltage mode that appears dominant in the DC voltages, defined as

$$\bar{v}_{dc} = \frac{1}{N_{st}} \sum_{n=1}^{N_{st}} v_{dc,n}$$

where N_{st} is the number of the converter stations in the grid.

The classical method was used to estimate the damping. For underdamped oscillations, the damping ratio is related to the logarithmic decrement and can be found from two adjacent peak values. As indicated in Figure 61a, using the identified first and second peak voltage values, denoted by ΔV_{peak1} and ΔV_{peak2}, respectively, the damping ration ζ is estimated by:

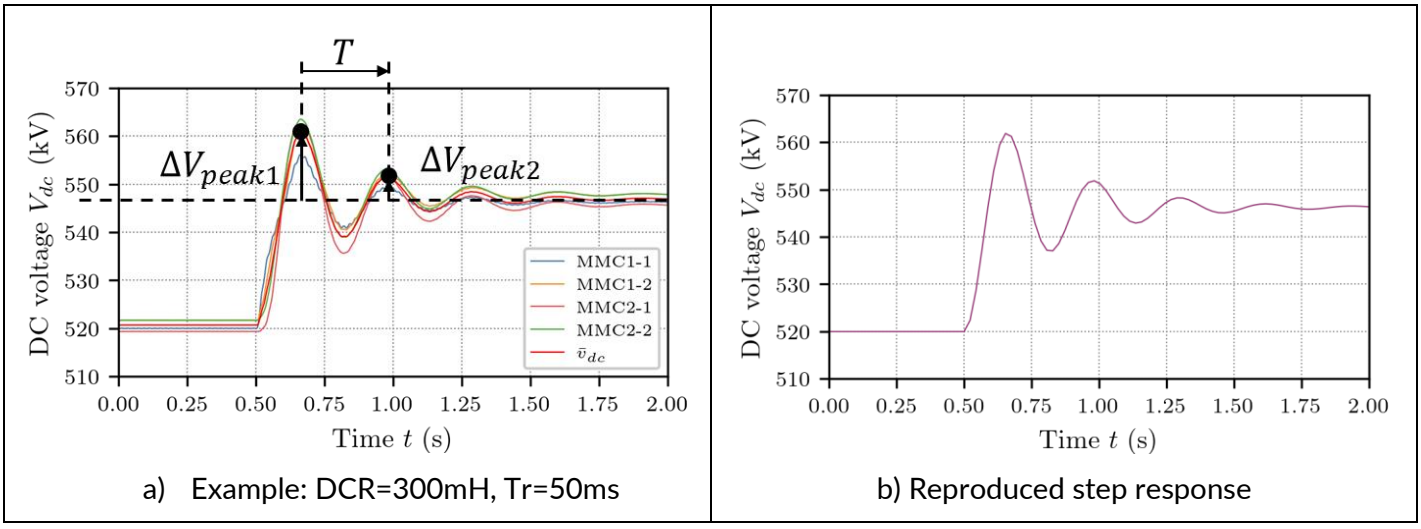
$$\zeta = \frac{1}{\sqrt{1 + \left(\frac{2\pi}{\ln \frac{\Delta V_{peak1}}{\Delta V_{peak2}}} \right)^2}}.$$

Then, using the damping ratio, the natural frequency ω_n can be derived by

$$\omega_n = \frac{2\pi}{T\sqrt{1+\zeta^2}}.$$

where T is the time between the two successive peaks.

From the estimated damping ratio and the natural frequency, the step response of the approximated second-order transfer function $E(s) = S^2 + 2\zeta\omega_n s + \omega_n^2$ is plotted in Figure 61b. It can be seen that very consistent results can be reproduced by the second-order transfer function, indicating that the damping ratio and natural frequency are accurately identified.



a) Example: DCR=300mH, Tr=50ms

b) Reproduced step response

Figure 61 Damping identification using STB result and reproduced step response

Using the method that was verified for accuracy, the values of the DCR size and T_r were varied to derive the damping ratio and the natural frequency in each case. The obtained results are summarized in Table 13. For AC systems, the damping ratio limit is typically set to 0.05 (5%) due to their oscillatory nature. The limit for DC systems is not standardized today, but is assumed here to be at least 0.10 (10%), and the values of the DCR size and T_r that satisfy it are colored blue and those that do not are colored red. For the sake of credibility, Figure 62 shows the simulation results for the three combinations positioned at the boundaries and the second-order response reproduced from the identified damping ratio and natural frequency. They show that the proposed methodology can identify the impact of DCR on system behavior for a given system topology using a relatively simple method, and that it can assist in specifying appropriate DC voltage controller parameters.

Table 13 Summary of the estimated damping ratios and natural frequency for different values of DCR size and Tr

DCR size\Tr	100 ms	50ms	30ms
300 mH	$\zeta = 0.23$ $\omega_n = 12.77$	$\zeta = 0.16$ $\omega_n = 19.98$	$\boldsymbol{\zeta = 0.12}$ $\boldsymbol{\omega_n = 24.26}$
600 mH	$\zeta = 0.20$ $\omega_n = 12.09$	$\boldsymbol{\zeta = 0.11}$ $\boldsymbol{\omega_n = 17.32}$	$\zeta = 0.08$ $\omega_n = 19.99$
900 mH	$\boldsymbol{\zeta = 0.17}$ $\boldsymbol{\omega_n = 11.50}$	$\zeta = 0.09$ $\omega_n = 15.65$	$\zeta = 0.05$ $\omega_n = 16.72$

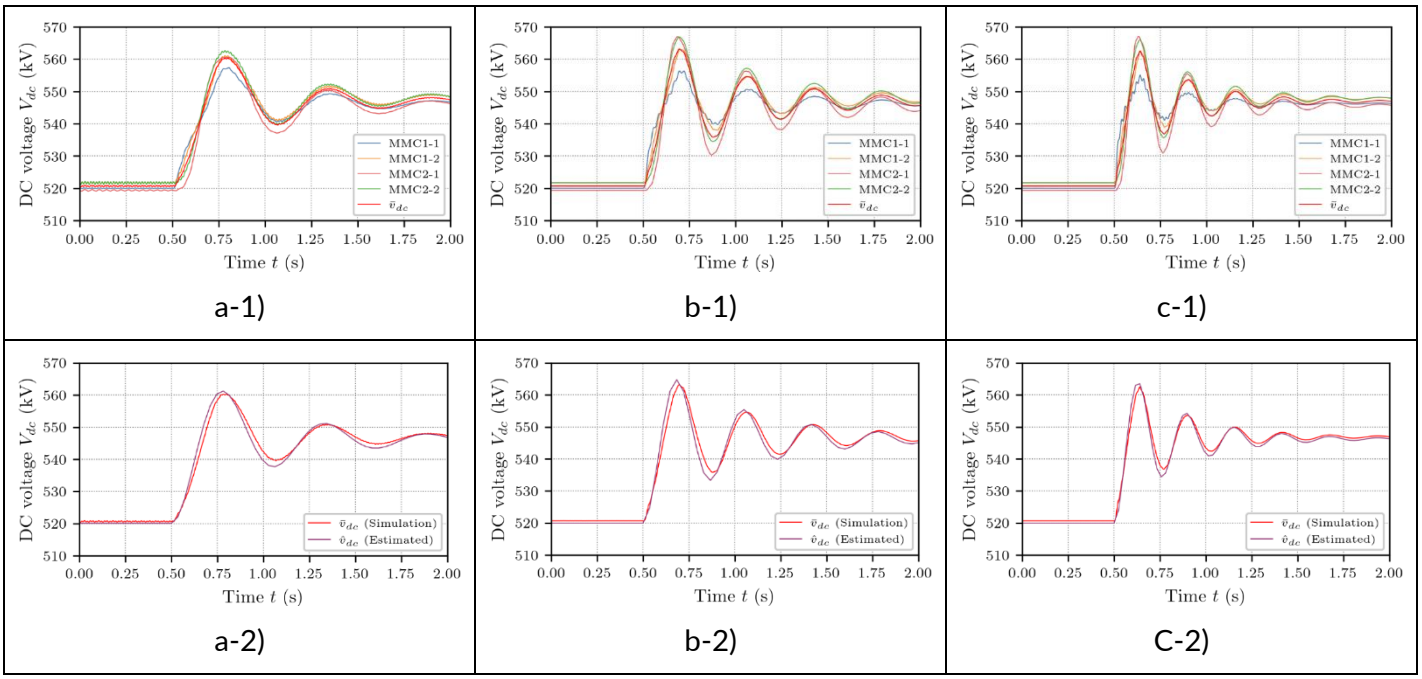


Figure 62 Simulation and estimation results of the combination positioned at the boundary (upper: voltages measured at PoC-DCs, lower: common DC voltage mode and the estimated second order response): a) DCR=900mH, Tr=100ms, b) DCR=600mH, Tr=50ms, c) DCR=300mH, Tr=30ms

6.2.4. FR and PR definition

The verification of the DC voltage controller should be done independently from the system and is recommended to be carried out by means of an externally verifiable step response time T_r. The DCR and the T_r of the fixed DC voltage controller can have significant impact on the dominant system mode (common DC voltage mode) and its damping. A step-by-step procedure for selecting T_r of the fixed DC voltage controller to ensure sufficient damping is proposed in this section. T_r should be set according to the DCR size.

The application of the fixed DC voltage control mode to a network larger than use case 1.1 is deemed impractical because it does not take advantage of headroom at other stations.

Table 14 Functional requirements related to fixed DC voltage control mode

ID	**Functional requirement**
General 22	The HVDC converter must be equipped with an independent controller allowing for regulating the DC voltage at the PoC-DC to a set-point by adjusting active power (or DC current or DC power) based on a set of specified parameters.

Table 15 Parameters related to fixed DC voltage control mode

ID	Symbol	Characteristic/Events	Range	Comments
35	Ts	time required for DC node voltages to settle to a new reference value after sudden changes, typically defined for a precision within 5% absolute distance to new reference value	$[30 - 120]$ ms	Adequate selection is needed considering the grid topology and the size of the DCR size
36	ΔUDC_S	Tolerance limit around the reference value. The total dead band = 2 ΔUDC_S	$[0.0015 - 0.0015 + \mathrm{X}]$ p.u.	This should be given by the steady-state switching harmonics generated by SM switching in steady-state plus the measurement error tolerance (The most accurate class is about 0.15%. [22])

6.3. Primary DC voltage control

For relatively large MTDC networks (i.e., more than three VSC units), the primary DC voltage control is typically achieved by the DC voltage droop control. In the literature, many variants in implementation exist, and the consensus has yet to be reached. A comparative study of different implementation schemes is out of the scope of this project and is a subject for future investigation.

6.3.1. Empirical understanding on the role of primary DC voltage control for disturbance management

The principal factors that determine the primary DC voltage control performance are: 1. The DC voltage droop control scheme, 2. The DC voltage droop gain, 3. The number of onshore converter stations in DC voltage droop control mode, and 4. external parameters such as DC grid impedance (including the cable resistance, reactance, and capacitance, as well as the MMC capacitance) and the size of DCRs.

Depending on the implementation scheme of the DC voltage droop controller, there are additional parameters that determine the DC-voltage behavior. Figure 63 depicts the different implementation schemes. The scheme used for this study and implemented in the use case corresponds to (d) in the figure, proposed in [23]. In [24], these five schemes were analyzed in terms of stability. The results suggest that scheme (d) exhibits more stable behavior and better robustness to a wider range of droop gains than scheme (a), at the expense of low frequency disturbance rejection ability. In the scheme (d), there are two internal control parameters, i.e. PI controller for DC voltage regulation: K_p^v and K_i^v. These parameters greatly affect the dynamic characteristics of droop-controlled converter station. The implications of those gains and the impact on the system dynamics are discussed in 6.3.4 in detail.

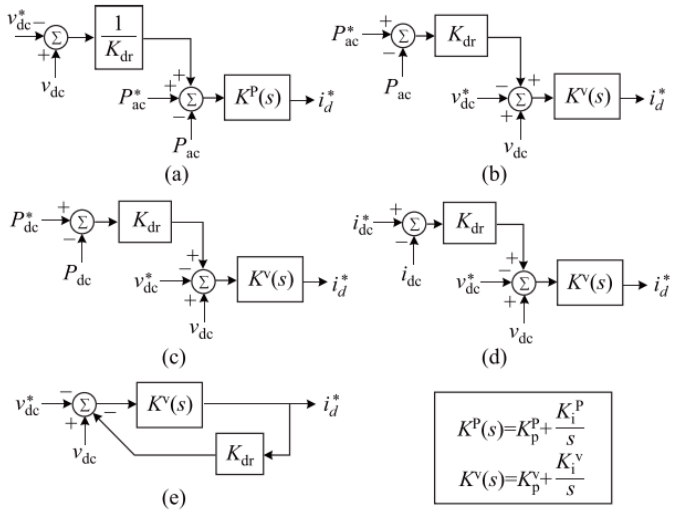


Figure 63 Different DC voltage droop implementation [24]

Regarding the droop parameter, the CENELEC report defines the droop as the change of active power in response to a deviation of the DC voltage from its reference value

$$s_{P\_UDC} = (\Delta U_{DC}/U_{DCnom}) / (\Delta P/Pn)$$

and the change of DC current in response to a deviation of the DC voltage from its reference value

$$s_{IDC\_UDC} = (\Delta U_{DC} / U_{DCnom}) / (\Delta I_{DC} / I_{DCnom})$$

As the power is given by the product of the voltage and current, while the voltage power relation is non-linear, the voltage current relation is linear. For more details on the difference between the two, see [25]. The latter relation, i.e. the linear voltage-current relation, is used for the simulations due to its compatibility with the aforementioned droop control scheme in Figure 63 (d). However, in the normal operating DC voltage range, the difference between the voltage-current characteristic and the voltage-power characteristic is not significant in terms of steady state. Therefore, for the sake of simplicity in developing the empirical understanding of the principle of droop control, the following section discusses with the voltage-power characteristics.

To determine the specification of the primary DC voltage control, the following two aspects should be considered: 1) disturbance management and 2) dynamic controllability requirements.

As the primary DC voltage control stems from the principle of the primary frequency control in AC systems, certain analogies can be made. In an AC system, its global characteristic is explained by the network power frequency characteristic λ_f defined as

$$\lambda_f = \frac{\Delta P_{dis}}{\Delta f} = \frac{1}{f_n}\left(\frac{S_{n1}}{k_{f1}} + \frac{S_{n2}}{k_{f2}} + \cdots \frac{S_{nN}}{k_{fN}}\right) + D$$

where

- ΔP_{dis} : power disturbance in the system in W
- Δf : post-contingency steady-state frequency deviation
- f_n : nominal frequency in Hz
- S_{nj} : rated power of the generating unit j in W
- k_{fj} : droop gain of the generating unit j in pu/pu
- D: aggregated self-regulating effect of load

The frequency droop k_f is commonly defined as the amount of frequency change which necessitates a change of the power output from 0 to 1 p.u. Typically, the minimum target value of λ_f is set as $\lambda_f > 15000$ MW/Hz , which confirms the 0.2 Hz deviation in case of 3000 MW, the dimensioning incident in CE, according to System Operator Guideline (SO GL) article 153(2b.i).

Similarly, the network power voltage characteristic λ_v can be defined for a DC system as

$$\lambda_v \approx \frac{\Delta P_{dis}}{\Delta v_{dc}} = \frac{1}{v_{dc_n}}\left(\frac{S_{n1}}{k_{vp1}} + \frac{S_{n2}}{k_{vp2}} + \cdots \frac{S_{nN}}{k_{vpN}}\right)$$

- ΔP_{dis} : power disturbance in the system in W
- Δv_{dc} : post-contingency steady-state DC voltage deviation
- v_{dc_n} : nominal DC voltage in V
- S_{nj} : rated power of the converter unit j in W
- k_{vpj} : droop gain (voltage-power characteristic) of the converter unit j in pu/pu

As there is no self-regulating effect in a DC system, the term representing the self-regulating effect is not considered. Note that, unlike the network power frequency characteristic of an AC system, the network power voltage characteristic only allows to grasp an approximate behavior of the DC voltage because of the voltage drop across the conductors that entails a discrepancy of the voltage measured at the different terminals.

The equation above indicates that if all stations have the same rating and are assigned the same droop gain, then, for a given disturbance (e.g., 1 GW), the post-contingent voltage deviation will be approximately determined by only two factors: droop gain and the number of stations in droop control mode in the DC grid.

In practice, of course, some additional constraints are imposed. For example, the pre-contingency operating state, in particular the pre-contingency operating power, determines the available headroom of the converter, beyond which the droop action is saturated. In addition, the above equation must take into account the actual number of stations that can contribute to the primary DC voltage, since blocked converters will no longer be able to contribute to primary DC voltage control.

Based on the above considerations, the following sections explain the implication of the droop parameters on the disturbance handling with simulations and describe the dimensioning methodology.

6.3.1.1. Impact of droop gain on the post-contingency voltage deviation

The following demonstrates by a simulation the influence of the droop gain on the post-contingency DC voltage deviation. The validated STB representing the use case 1.1, depicted in Figure 64, was used. The size of DCR was set to 300 mH as a first starting point for the analysis. The initial operating point is summarized in Table 16. The considered scenario here is the sudden loss of power injection from the wind farm connected to the offshore station MMC2-2 without converter blocking (e.g., this can happen in case of a fault at the connection point to the wind farm) at=0.5s. Then, the same simulation was repeated with the droop gain of MMC 1-1 and 2-1 changed from 0.01 to 0.20.

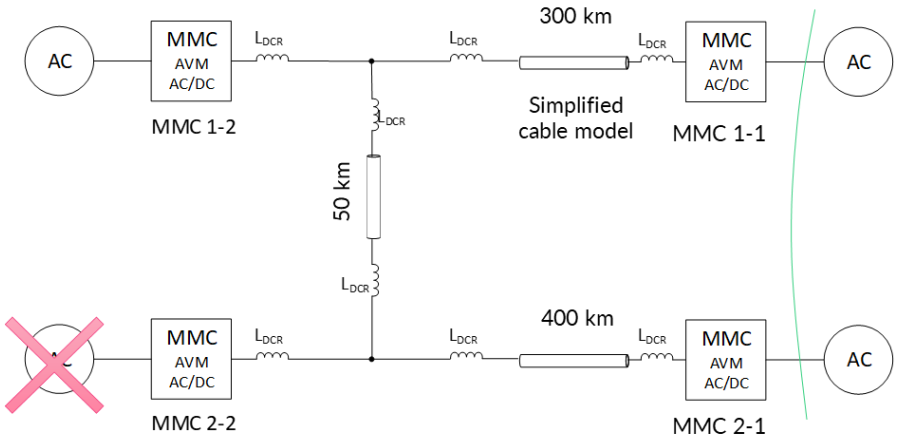


Figure 64 Studied case: Impact of droop gain

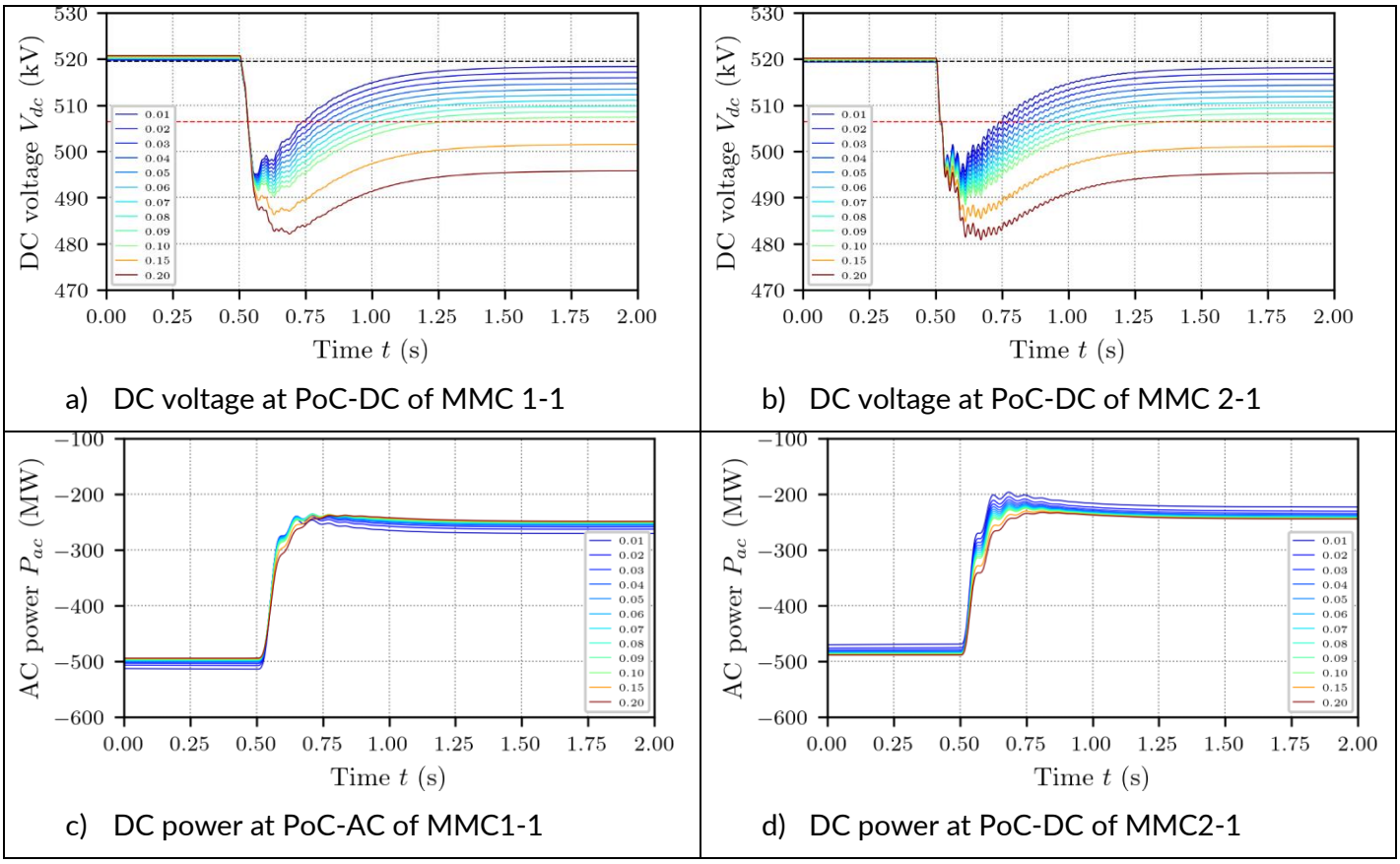
Table 16 Initial operational set-points

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain
MMC 1-1	Vdc droop control	-485	519.5	0.01~0.20
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Vdc droop control	-485	519.5	0.01~0.20
MMC 2-2	Fixed Ac power	+500	N/A	N/A

The obtained results are shown in Figure 65. Figure 65a and b show the DC voltages measured at PoC-DCs of the onshore stations. As seen, the sudden drop in power injection caused from MMC2-2 results in a temporary voltage drop, but the primary DC voltage containment process by the droop control leads to in a smooth transition to the post-contingency steady state. The post-contingency steady-state DC voltage deviation is proportional to the droop gain. The dashed red line indicates a deviation by -2.5 % from the initial voltage level. According to the expression below,

$$\Delta v_{dc} \approx \frac{\Delta P_{dis}}{\lambda_v} = \frac{v_{dc_n}}{\left(\frac{S_{n1}}{k_{v1}} + \frac{S_{n2}}{k_{v2}}\right)} \Delta P_{dis},$$

the post-contingency DC voltage deviation can be approximately -2.5 % in case of a droop value of 0.10. Although slight discrepancy is observed due to the voltage drop across the cable, the results confirm the validity of the approximation by the network power voltage characteristic. Figure 65c and d show the DC power at PoC-DCs. The smaller the droop gain, the more sensitive to the resistive voltage drop in the grid, which affects the power contribution. By increasing the droop gain, this effect is reduced, and the power is distributed more equally among the droop-controlled stations. It should be noted here that the dynamic behavior until the system reaches the post-contingency steady state is highly dependent on the implemented droop scheme and its parameters. This point will be discussed in more detail in Section 6.3.4.



a) DC voltage at PoC-DC of MMC 1-1

b) DC voltage at PoC-DC of MMC 2-1

c) DC power at PoC-AC of MMC1-1

d) DC power at PoC-DC of MMC2-1

Figure 65 Simulation results: impact of droop gain on the post-contingency voltage deviation

6.3.1.1. Impact of the size of disturbance on the post-contingency voltage deviation

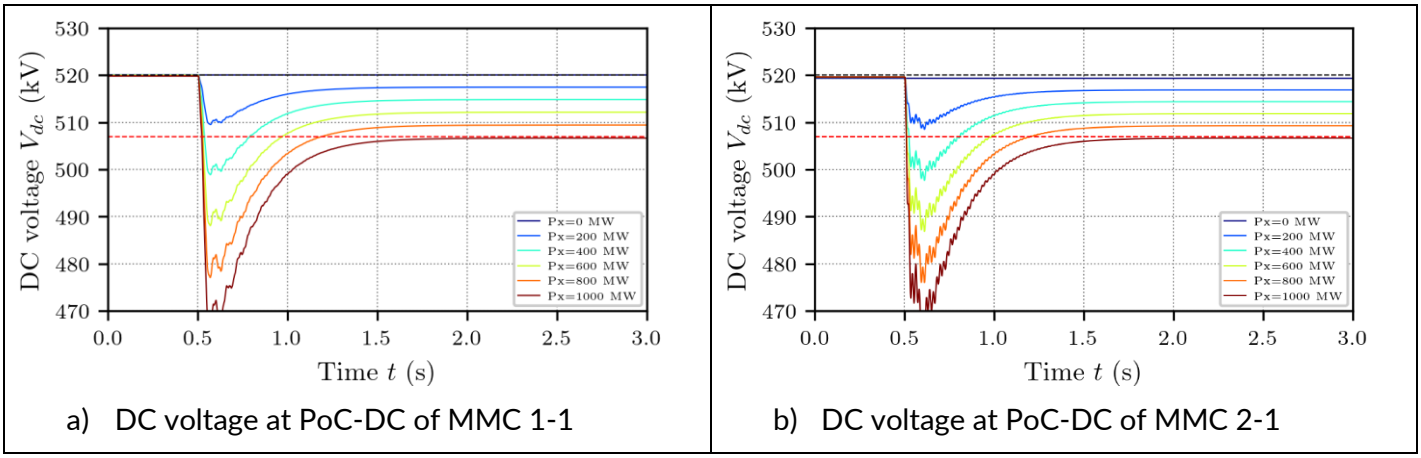
Using the same simulation set-up, the following demonstrates the impact of the magnitude of the disturbance on the post-contingency states.

Here, the droop gain is fixed to 0.05. While the set-points of the onshore stations are kept the same as the previous simulation, the initial operating active power of the offshore stations are varied as

- MMC 1-2: $1000 - P_x$
- MMC 2-2: P_x

where $P_x = [0{\sim}1000]$ MW. Since the total power injection from the offshore stations is kept the same, the two onshore stations equally receive power in the pre-contingency state. For each case, the power injection from MMC2-2 is forcibly reduced to zero at t=0.5s.

Figure 66 shows the obtained results of the DC voltages measured at PoC-DCs of MMC1-1 and 2-1. As the definition of the network power voltage characteristic indicates, the deviation of the DC voltage after a contingency is proportional to the magnitude of the disturbance. This implies that the maximum disturbance size (dimensioning incident) is an important factor in determining the droop parameters.



a) DC voltage at PoC-DC of MMC 1-1

b) DC voltage at PoC-DC of MMC 2-1

Figure 66 Simulation results: Impact of size of disturbance on the post-contingency voltage deviation

6.3.1.1. Special consideration

The results presented so far show a simple linear relationship between droop parameter and post-contingency steady-state voltage. However, unlike AC grids, where hundreds of units contribute to primary frequency control, the contribution required of each converter station in the MTDC grid with a very small number of converters is significant. This means that the outage of a converter station that is expected to contribute to the primary DC voltage control has a significant impact on the primary DC voltage containment process. Furthermore, the upper limit to which a converter can contribute to the primary DC voltage control is limited by the maximum power capacity, and hence, the available headroom capacity of the converter.

To demonstrate the importance of these special considerations, the following simulations have been performed for the case shown in Figure 67. Since the loss of an offshore converter station does not reduce the number of converters equipped with a DC voltage droop, the scenario considered here is the unfavorable situation where one of the onshore converter stations lost its power transfer capability. When the station can no longer contribute to the primary DC voltage control, the burden falls on the remaining station.

The operating set-points are summarized in Table 17. Two different operating conditions are considered: one with power injections from the offshore stations of 500 MW each, and the other with 750 MW each.

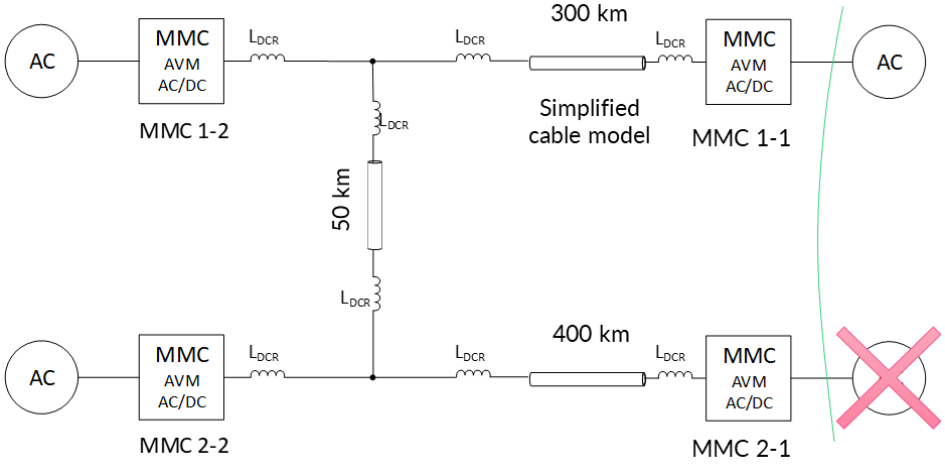


Figure 67 Studied case: Impact of special consideration

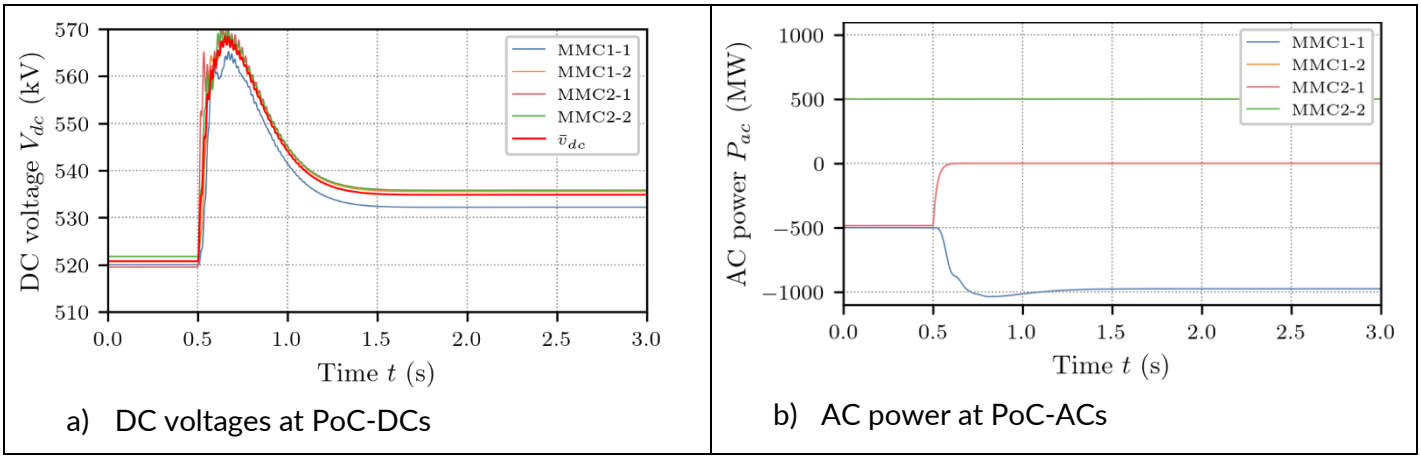
Table 17 Initial operational set-points for the studied case: Impact of special consideration

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain
MMC 1-1	Vdc droop control	-485 or -735	519.5	0.05
MMC 1-2	Fixed AC power	+500 or +750	N/A	N/A
MMC 2-1	Vdc droop control	-485 or -735	519.5	0.05
MMC 2-2	Fixed Ac power	+500 or +750	N/A	N/A

Figure 68a shows the DC voltage at the PoC-DC of each station. Their average, $\bar{v}_{dc}$, is shown in red. The blocking of MMC 2-1 leads to an immediate loss of the power extraction of 500 MW. This loss needs to be compensated by the remaining onshore station, MMC 1-1. With the assigned drop of 0.05, the post-contingency DC voltage deviation

$$\Delta v_{dc} \approx \frac{\Delta P_{dis}}{\lambda_v'} = \frac{v_{dc_n}}{\left(\frac{S_{n1}}{k_{v1}}\right)} \Delta P_{dis},$$

gives approximately 2.5 %, which corresponds to the dashed line. Figure 68b shows the AC power of each station. It can be seen that MMC1-1 has accomplished the primary DC voltage containment process without exceeding the maximum power capacity because it had a sufficient headroom in the initial condition.



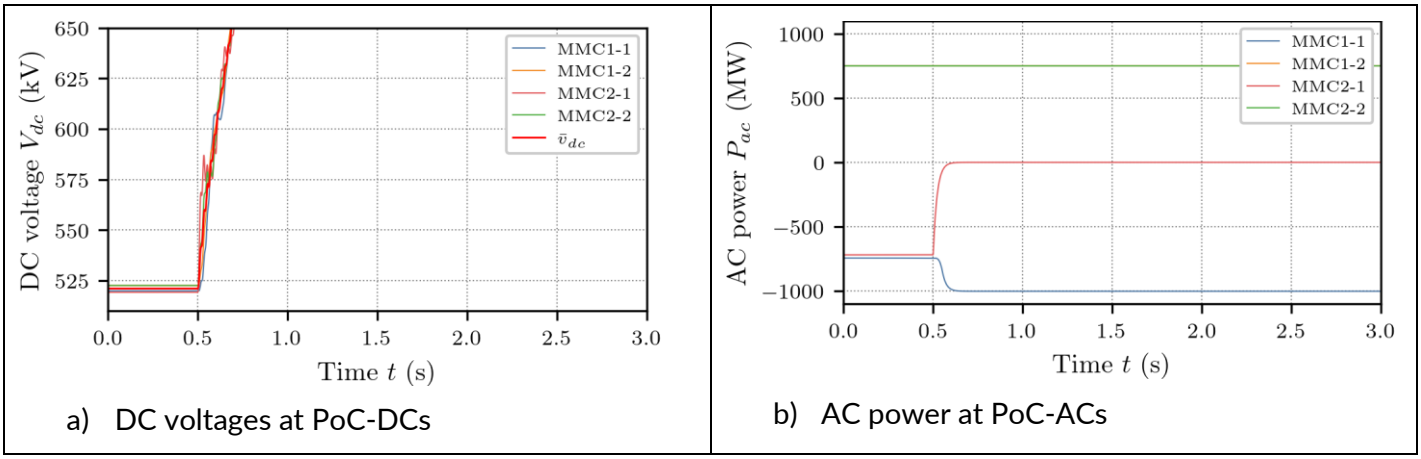
a) DC voltages at PoC-DCs

b) AC power at PoC-ACs

Figure 68 Simulation results: Impact of special consideration (Case 1)

Contributions to the primary DC voltage control can be only possible if the maximum power of the converter is not exceeded. Therefore, the following presents a similar simulation but with a smaller available headroom in the initial state. The operating set-points are as summarized in Table 17.

The obtained results are shown in Figure 69. The power of MMC 1-1 is saturated at the maximum power capability because it does not have enough headroom to compensate for the loss of power extraction due to the blocking of MMC 2-1; the DC grid has lost the control of the DC voltage, and the DC voltage rises uncontrollably as shown in Figure 69a. This clearly shows the need for voltage limiting by DBS or other features, which are discussed in 0



a) DC voltages at PoC-DCs

b) AC power at PoC-ACs

Figure 69 Simulation results: Impact of special consideration (Case 2)

6.3.2. Methodology for specifying the droop parameters for disturbance management

To summarize the results of the previous sections,

- → The post-contingency steady-state DC voltage deviation can be well approximated by the simple expression.
- → The deviation of the post-contingency steady-state DC voltage deviation is proportional to the magnitude of the disturbance.
- → Only the loss of the converter stations that can contribute to the primary DC voltage control should be considered for the estimation of the post-contingency steady-state DC voltage deviation.
- → If compensation is not possible due to headroom availability constraints, voltage limitation by Dynamic Braking System (DBS) is required.

Based on the above conclusions, the following proposes the methodology for droop parameter specification.

First, the upper and lower limits of the post-contingency voltage deviation, denoted by $\Delta\bar{v}_{dc}^{Max}$ and $\Delta\bar{v}_{dc}^{Min}$, are set. Since the DC voltage at each node varies depending on the power flow conditions, these are only indicated values to be imposed on the average value. Here, two values are assumed, $\Delta\bar{v}_{dc}^{Max,Min} = \pm 5\%$ and $\pm 10\%$.

Next, the largest magnitude of the power disturbance, namely, the dimensioning reference incident P_{RI}, that can occur in the system is determined. In the AC systems, this value is specified for each synchronous system, e.g. 3000 MW in CE corresponding to the trip of two largest generation units, according to System Operator Guideline (SOGL) article 153(2b.i). However, a more in-depth analysis is needed for the MTDC grid, which consists of a relatively small number of stations. The provided use case assumes a bipolar configuration with DMR[3]. Since a change in power flow in one pole does not directly affect other pole in steady-state, the dimensional incident can be analyzed considering only one pole. The maximum power disturbance should indeed consider the protection strategy for each type of fault. Here assumes the selective protection strategy, and the converter blocking constraints for each type of fault are provided in Table 46. The maximum power imbalance in post-contingency steady-state that may occur considering all possible fault must be considered. In addition, if an incident results in a system split, the power disturbance for each system after the split is counted. For example, an interconnector trip that is transmitting 1 GW will appear as a disturbance of 1 GW on one side and -1 GW on the other.

Table 18 summarizes the prospective power disturbances in a pole and their maximum magnitude for use case 1.1. It is important to note that for disturbances of the same magnitude, the availability of the fewer converter stations that can contribute to the primary DC voltage control means a more severe scenario.

[3] It is worth to note that operation of the grid in rigid bipole is not considered in this study.

Table 18 Prospective disturbance to be considered for the specification of droop parameters

N.	Prospective sources of disturbance	Use case	Maximum disturbance that can be seen by the remaining part of the system (in each system after the split, if a system split occurs)	Minimum number of remaining converters available to compensate for the disturbance (in each system after the split, if a system split occurs)	Comment
1	Busbar fault (primary & backup)	Use case 1.1, 1.2	$\pm 1\mathrm{GW}$	1	A busbar fault (regardless of primary or backup sequence) results in a loss of the connected offshore station, interconnector, and the spoke. At least one onshore station is available for disturbance compensation in the system that remains.
		Use case 2	$\pm 2\mathrm{GW}$	2	A particular consideration is needed for fault in busbar in ring topology. These can cause up to $\pm 2\mathrm{GW}$ of disturbance to the rest of the system.
2	PtG fault in an interconnector	Use case 1.1 and 1.2	$\pm 1\mathrm{GW}$	1	Fault in interconnector and eventual disconnection will inevitably result in a system split. For each system after the system split, one onshore station to compensate for the disturbance is expected.
		Use case 2	$\pm 2\mathrm{GW}$	2	A particular consideration is needed for faults between busbars. These can cause up to $\pm 2\mathrm{GW}$ of disturbance to the rest of the system.
3	Blocking of an onshore station	Use case 1.1, 1.2 and 2	$\pm 1\mathrm{GW}$	1	
4	Blocking of an offshore station	Use case 1.1, 1.2 and 2	$-1\mathrm{GW}$	2	
5	PtG fault in a spoke	Use case 1. and 1.2	$\pm 1\mathrm{GW}$	1	
		Use case 2	$-2\mathrm{GW} \sim +1\mathrm{GW}$	2	In case of back up sequence.
6	AC fault at the connection of an onshore converter without blocking	Use case 1.1	$\pm 2\mathrm{GW}$	0	A particular consideration is needed for in case of an AC fault at the bus connecting MMC 1-1 and 2-1. As no station can evacuate the power, DBSs need to be activated
		Use case 1.2 and 2	$\pm 2\mathrm{GW}$	2	

In a radial topology (Use case 1.1 and 1.2), a fault may cause the system to split. The power disturbance seen by each system after the split is limited to the power that was exchanged through the fault location. Therefore, the power that must be compensated by the primary DC voltage control is limited to a maximum of $\pm 1\text{GW}$. On the other hand, in the meshed use case, more than 1 GW of disturbance may have to be compensated by the primary dc voltage control. However, as mentioned earlier, the more converter stations that can contribute to primary dc voltage control, the less power each converter must compensate for because the burden is distributed. Therefore, the maximum burden that single converter station must compensate for is limited to $\pm 1\text{GW}$. From this, it can be concluded that reference incident value $P_{RI} = \pm 1\text{GW}$ can be used as the dimensioning value. Then, the droop parameters can be specified as the specified upper and lower limits of the post-contingency voltage deviation by:

$$k_v \leq \frac{\min\{|\Delta\bar{v}_{dc}^{Max}|, |\Delta\bar{v}_{dc}^{Min}|\}}{\frac{P_{RI}}{S_n}}.$$ [4]

And this gives $k_v = 0.05$ for $\Delta\bar{v}_{dc}^{Max,Min} = \pm 5\%$, and $k_v = 0.10$ for $\Delta\bar{v}_{dc}^{Max,Min} = \pm 10\%$. [5]

6.3.3. Empirical understanding on dynamic controllability requirements

The previous section described the specification of the droop parameters that determines the DC voltage containment process by the primary DC voltage control. This section describes the controllability requirements for the DC voltage control. In general, the DC voltage droop control takes the DC voltage set-point and active power set-point as inputs (either P_{ac}^*, P_{dc}^* or I_{dc}^* depending on the droop scheme). The difference between P_{ac}^* and P_{dc}^* (or I_{dc}^*) depends on how the loss inside the MMC is taken into account in deriving the setpoints. Here, these references are collectively referred to as active power.

For the aforementioned two controllability aspects, the feasibilities and limitations of the DC grid consisting of the MMCs contributing to the primary DC voltage control are discussed separately below.

6.3.3.1. Controllability of DC voltage

Under droop control with a given droop parameter, the equilibrium operating point is uniquely determined from the set-points of each converter (or imposed power injection in case of connection to wind farm, etc.) and the grid impedance. A change in setpoint means a change in this equilibrium point. In droop control, the difference between the DC voltage setpoint and the measured value is seen as the control error. From a control point of view, an increase of the DC voltage setpoint of a station is equivalent to a decrease of the measured DC voltage. The DC voltage droop controller, as a result, injects more power to the DC side to support the DC grid voltage. For other stations, this will simply appear as a disturbance. The droop controllers of these stations now act to extract more power from the DC side to contain the DC voltage rise. Therefore, an uncoordinated change in

[4] For simplicity, the expression assumes that all stations are rated at the same power Sn. For stations with different ratings, it is necessary to convert the droop gain to account for their rated power so that the P-Vdc characteristics in SI unit are the same.

[5] Note that if Delta Vdc max = 0, then it leads to droop gains to be zero, resulting in the situation more than one stations controlling the voltage at PoC-DC to the respective reference value in a similar way as the fixed DC voltage control mode. This means that no onshore stations exert active power controllability.

the DC voltage setpoint will appear as a disturbance to the system. Therefore, an adjustment of the DC voltage setpoint requires coordination through the DC grid controller.

The following demonstrates a coordinated change of the set-points of DC voltage by simulation. As in the previous section, the STB developed using the AVM AC/DC and the simplified cable models is considered, shown in Figure 70. The set-points are summarized in Table 19. For simplicity, the same DC voltage setpoint is given to MMC1-1 and MMC2-1 here; the setpoint is stepped up by 10% at t=0.5s, and at t=1.5s, it is stepped down to 90% of the initial value (0.9 p.u.).

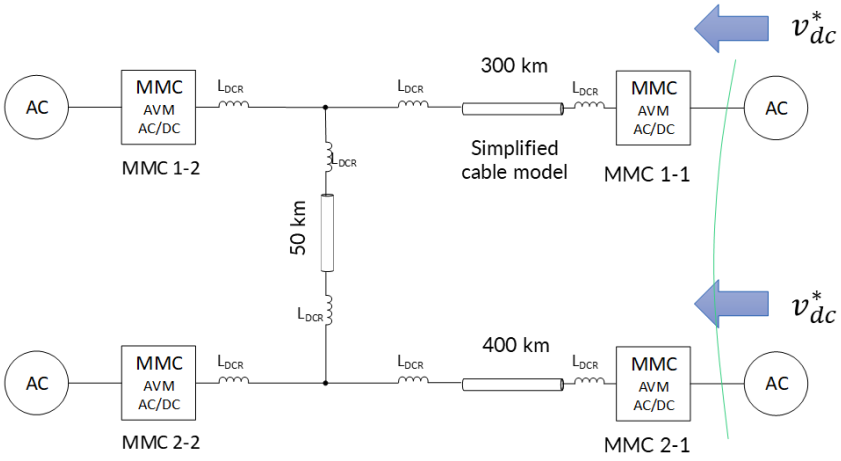


Figure 70 Studied case: coordinated DC voltage set-points change

Table 19 Initial operational set-points

	Operating mode	Active power set-point P_{ac}^* [MW]	DC voltage set-point V_{dc}^* [kV]	Droop gain
MMC 1-1	Vdc droop control	-485	$519.5 \rightarrow 572 \rightarrow 467$	0.05
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Vdc droop control	-485	$519.5 \rightarrow 572 \rightarrow 467$	0.05
MMC 2-2	Fixed Ac power	+500	N/A	N/A

The results are shown Figure 71. As observed in Figure 71a showing the DC voltages measured at PoC-DC of each station, the voltages smoothly shift to the dispatched set-point levels of $\pm 10\%$ of the initial voltage level, indicated by the dashed lines. Figure 71b shows the DC power. As observed, some power fluctuations occur during the transient, but the DC power will converge to the initial power level as the DC voltage reaches a steady state.

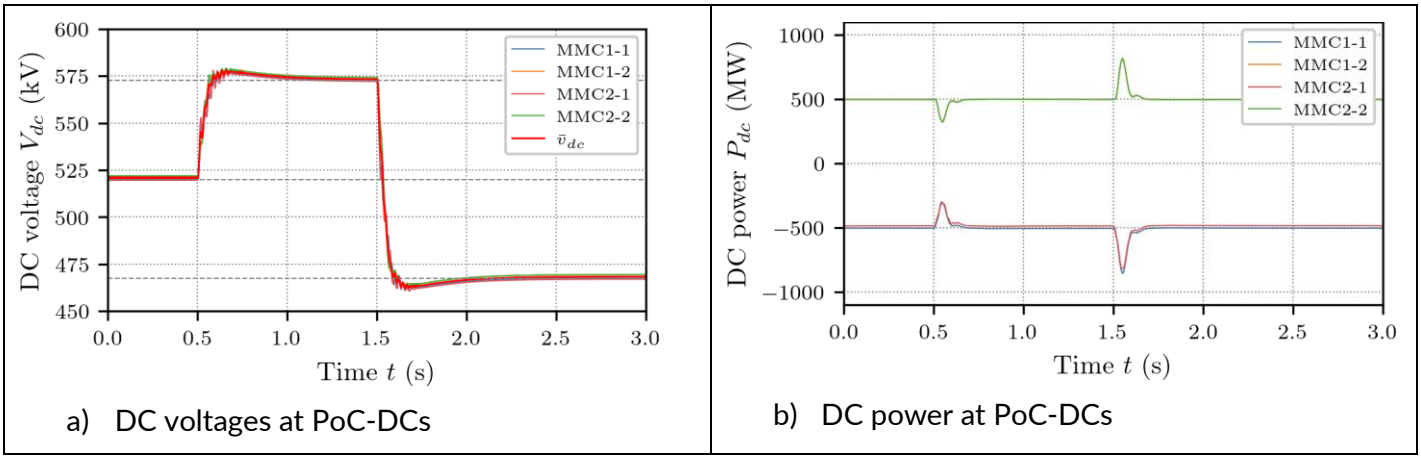


Figure 71 Simulation results: Controllability of DC voltage

The obtained results clearly indicate the feasibility of a change in the operating level of the DC grid voltage through a coordination of the DC voltage set-points of the stations by the DC grid controller. The validity of the new set-points must be judged at the DC grid controller level.

The dispatch of new set-point values from the DC grid controller incurs a latency due to communication. In the simulations, step changes were imposed to demonstrate the feasibility. However, in practice, the DC voltage set-points must be changed with sufficient ramp speed with continuous monitoring so that the difference in latency does not render the system unstable.

6.3.3.1. Controllability of active power

As in the discussion of DC voltage controllability in the MTDC grid, the controllability of active power leads to different conclusions depending on the presence or absence of coordination. In addition, it is necessary to distinguish between the controllability of active power in the DC voltage droop mode and the controllability of the active power in the active power control mode. The possible combinations to be considered in this section are summarized in Table 20.

Table 20 Possible combinations to be distinguished in the discussion of active power controllability

	Presence or absence of coordination	
Control mode of the concerned station	Absence of coordination	Presence of coordination
Power control mode	Uncoordinated change of set-point of active power in power mode	Coordinated change of set-points of active power in power mode
DC voltage droop mode	Uncoordinated change of set-point of active power in droop mode	Coordinated change of set-points of active power in droop mode

Uncoordinated change of the set-point of active power of the station in power control mode

This case is considered as the reference case. Assuming a stable initial condition, at some instant, only the active power setpoint of the station in power control mode is changed. The active power response should be determined by the design and tuning of the active power controller. The criterion for the adequacy considered here is that the set-point should be reached within 200 ms, in accordance with the post-fault active power recovery requirement in the NL grid code.

The same STB as shown in Figure 71 was used for demonstration. The station in question is MMC2-1, which is intentionally set to fixed active power control mode. At t=0.5s, the set-point of active power is changed from -485 to -985 MW (-500 MW step change).

Table 21 Initial operational set-points for the studied case: Uncoordinated change of set-point of active power in power mode

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain s
MMC 1-1	Vdc droop control	-485	519.5	0.05
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Fixed AC power	-485 →-985	N/A	N/A
MMC 2-2	Fixed Ac power	+500	N/A	N/A

The obtained results of the DC voltages, and AC power are shown in Figure 72a and b, respectively. The change in the active power set-point is not coordinated, and thus, the change in active power extraction is compensated by the other station in DC voltage droop mode, i.e. MMC1-1. Figure 72c and Figure 72d show the zoom of the active power response of MMC 2-1 and MMC 1-1, respectively. As expected, the active power controller of MMC 2-1 in fixed active power control is configured to reach the set-point within approximately 200 ms.

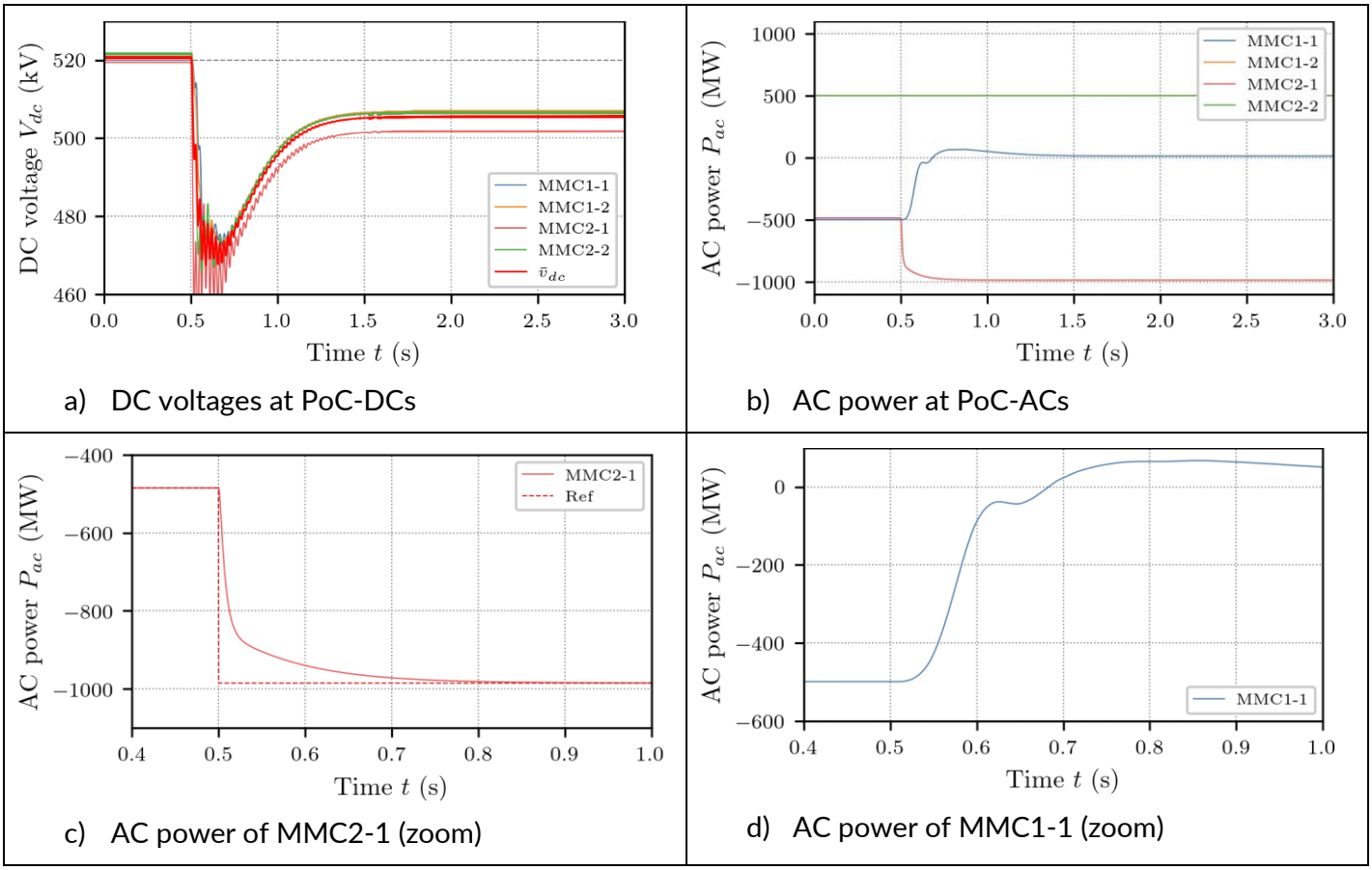
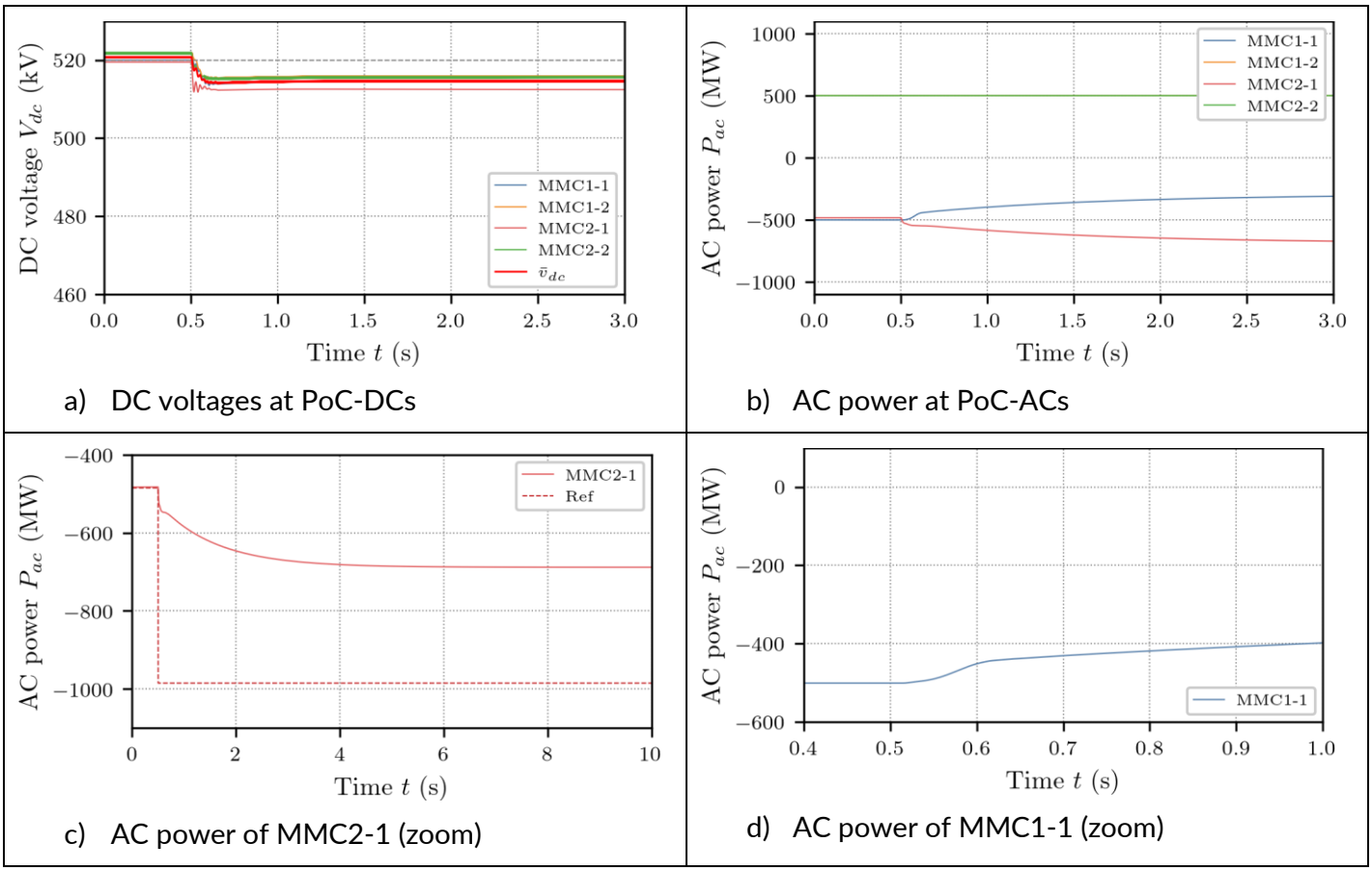


Figure 72 Simulation results: Uncoordinated change of set-point of active power in power mode

Uncoordinated change of set-point of active power of the station in droop control mode

In this simulation, MMC 2-1 is set to droop control mode and the same simulation as in the previous simulation is performed. The results are shown in Figure 73. Figure 73a and b show the DC voltages and AC active power, respectively. It can be seen that the behavior is completely different from the previous case. Figure 73c and d show the zoom of the active power response of MMC 2-1 and MMC 1-1, respectively. Obviously, MMC2-1 is not able to track the new reference value at all. Therefore, the corresponding power change in MMC 1-1 remains small.

The cause of the discrepancy between the reference and the actual value of the power in MMC 2-1 is that an uncoordinated change of the active power setpoint will inevitably trigger its own DC voltage droop controller. Therefore, the actual output is the set value plus the effect of droop control (in the opposite direction of the set-point change).



a) DC voltages at PoC-DCs

b) AC power at PoC-ACs

c) AC power of MMC2-1 (zoom)

d) AC power of MMC1-1 (zoom)

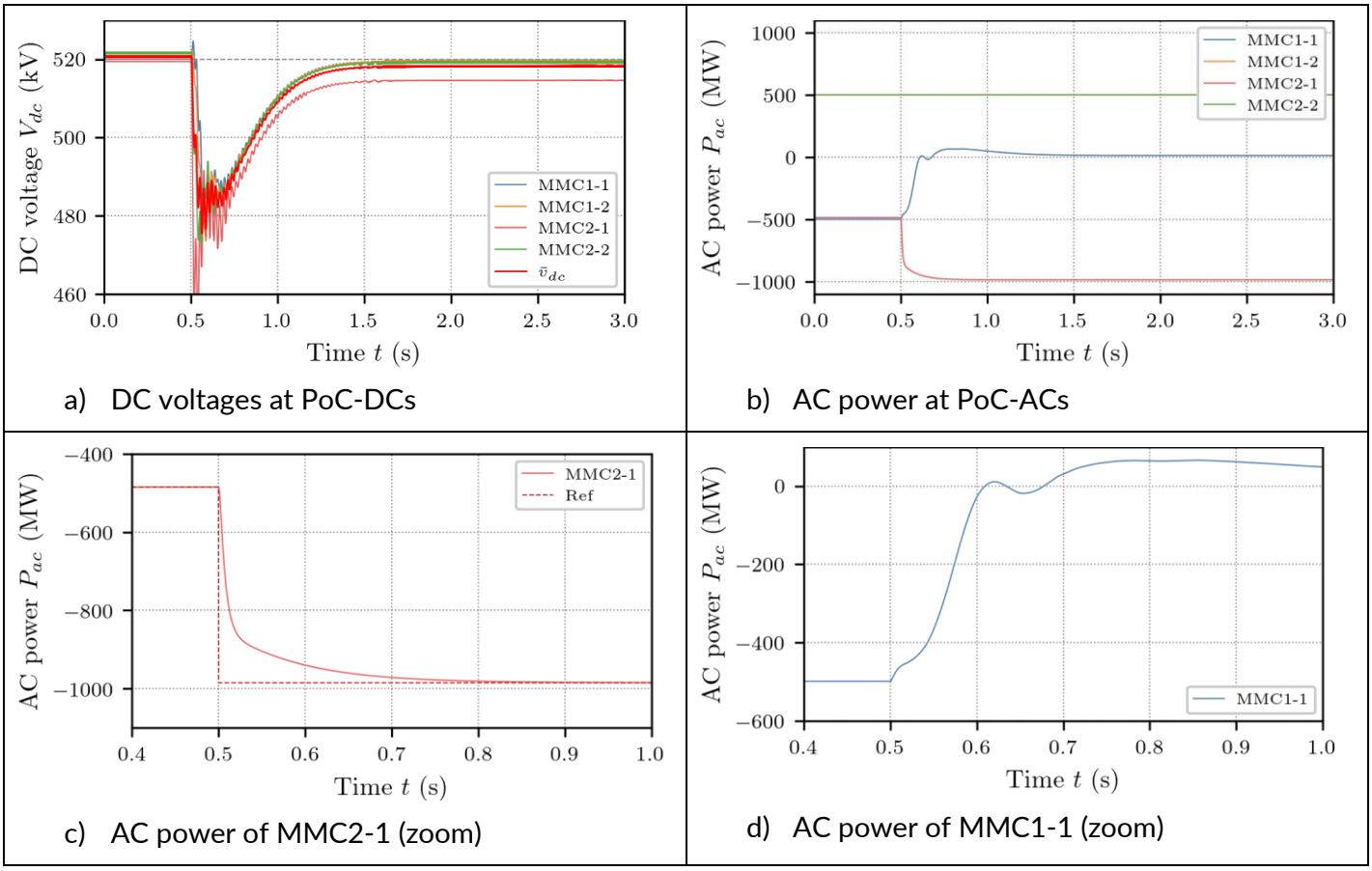
Figure 73 Simulation results: Uncoordinated change of set-point of active power in droop mode

Coordinated change of set-points of active power of the station in power control mode

Coordinated change of the active power setpoint here refers to changing the setpoint of one station while at the same time changing the setpoints of another station to compensate for the first one. Thus, changing the active power setpoint here is not just a matter of one station, but also a matter of to which station the active power is transmitted.

The same set-up is used for simulation. At t=0.5s, the set-point of MMC2-1 is step changed by -500 MW while at the same time, the set-point of MMC1-1 in DC voltage droop mode is increased by +500 MW.

The obtained results are shown in Figure 74. A clear difference from the uncoordinated change of set-point is that, in the steady-state, the DC voltages return to almost the same level as the initial state. This means that coordinated active power set-point change is able to prevent the disturbance from inducing a permanent change in the DC voltage.



a) DC voltages at PoC-DCs

b) AC power at PoC-ACs

c) AC power of MMC2-1 (zoom)

d) AC power of MMC1-1 (zoom)

Figure 74 Simulation results: Coordinated change of set-point of active power in power mode

Coordinated change of set-points of active power of the stations in droop control mode

Lastly, a coordinated change in the active power setpoint of the stations in droop mode is demonstrated in the following. To clarify the impact of this difference, the same simulation was used as in the case of coordinated change with the initial operating set-points shown in Table 22.

Table 22 Initial operational set-points for the studied case: Coordinated change of set-point of active power in droop mode

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain
MMC 1-1	Vdc droop control	-485 →+15	519.5	0.05
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Vdc droop control	-485 →-985	519.5	0.05
MMC 2-2	Fixed Ac power	+500	N/A	N/A

Figure 75 show the obtained results. As seen in Figure 75a, there is no significant fluctuations in the DC voltages. This is because, unlike previous cases, MMC1-1 and MMC2-1 are both in the DC voltage droop mode and have the same dynamic characteristics in this simulation. Therefore, it can be said that harmonizing the dynamic characteristics is beneficial from the viewpoint of reducing the DC voltage fluctuation of the system.

On the other hand, there is a clear difference in the response of active power compared to the previous case. As seen in Figure 75c, compared to the previous simulations, the response time for active power is more than ten times slower than the previous case with coordinated change of set-points of active power of the stations in active power control mode. This response speed is deemed unacceptable in terms of other DC and AC ancillary service requirements. It should be noted, however, that this is solely a matter of design and tuning of the implemented droop controller. In the following section, the impact of the tuning of the droop controller parameters on the active power response and the dynamic response specifications are discussed. On the other hand, the deviation between the active power setpoint and the actual active power in steady state is an inherent problem of DC primary DC voltage control based on the droop control. Unlike frequencies in AC systems, the voltage at each node of the DC grid does not take the same value. Moreover, any change in the power flow in the MTDC grid entails the change in the voltage drop across the grid. Even if the active power set-points are changed in a coordinated manner, it does not mean that the DC voltage set-points given initially will be appropriate for the new desired power flow. Therefore, each station in the droop mode will seek the equilibrium point at the expense of the error between the set point and actual active power output through the droop controller. Possible solutions to this problem could be to use power flow analysis to derive optimal set-points or to effectively utilize dead bands in the droop characteristics. The former option will be discussed in more detail in the dedicated sections, i.e. 6.3.3.2 and 6.5.

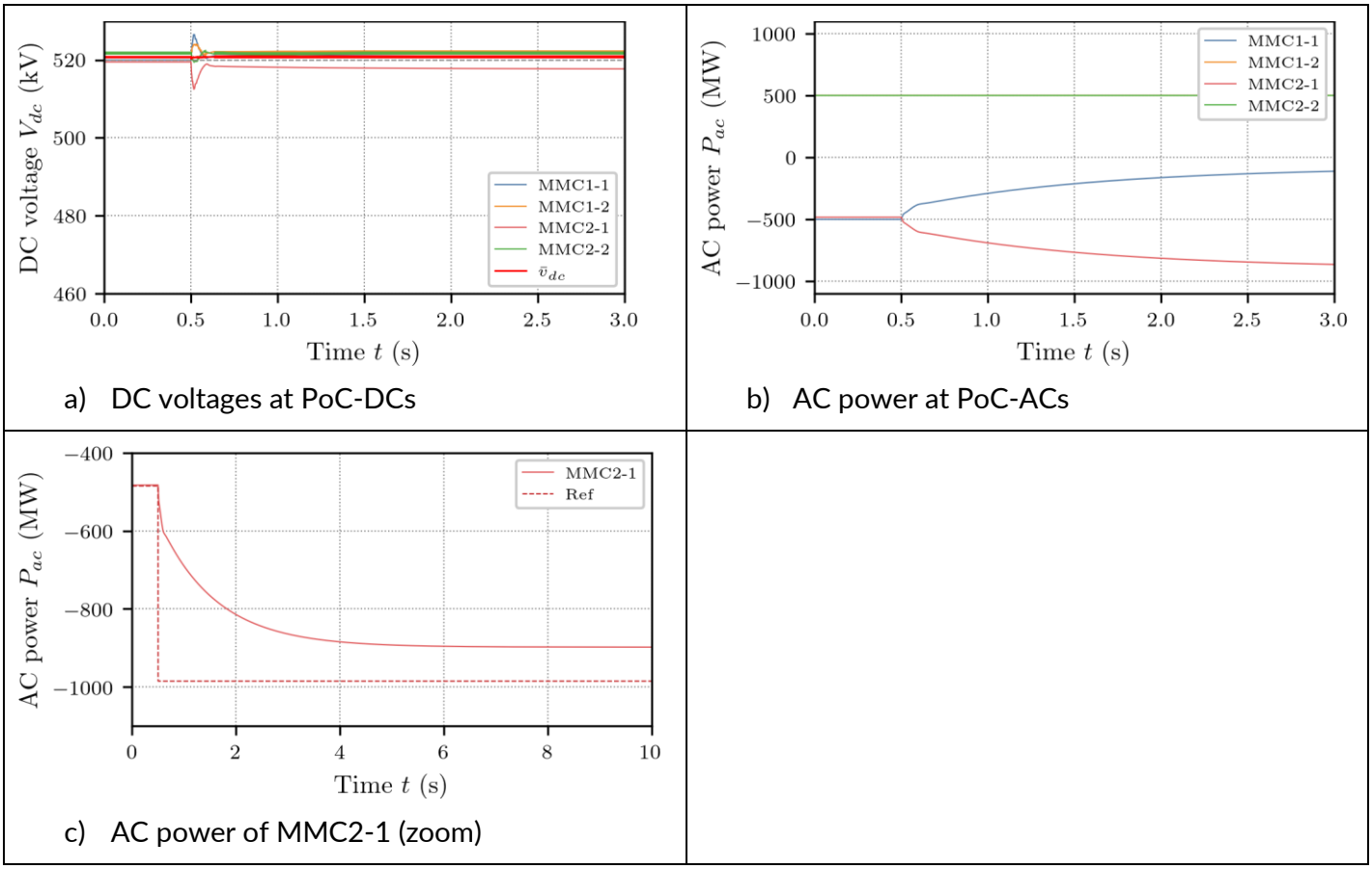


Figure 75 Simulation results: Coordinated change of set-point of active power in droop mode

6.3.3.1. Dynamic response of DC voltage droop mode

The design and tuning of the droop controller have a significant impact on the controllability of the active power. It has been agreed with the client that a comparative study of the possible droop controller design is a future subject. Therefore, this section focuses on the scheme under verification shown in Scheme (d) in Figure 63.

In the droop scheme under consideration, there are two internal control parameters subject to tuning, i.e. proportional and integral gains of the PI control for DC voltage regulation, denoted by K_p^v and K_i^v, respectively. Since it is impractical to exhaustively test all possible combinations of these two variables, the classical pole placement method is adopted for the tuning while considering only the response speed T_r as variable.

Taking advantage of the similarity between the fixed DC voltage control and the PI controller in the selected droop scheme, the gains are set using the same procedure as in Section 6.2.1.

Applying the pole placement method, the PI controller gains are derived by fitting the closed loop transfer function by selecting the gains as:

$$K_p^v = 4\zeta\omega_n H_{mmc}$$
$$K_i^v = \frac{1}{T_i^v} = 2\omega_n^2 H_{mmc},$$

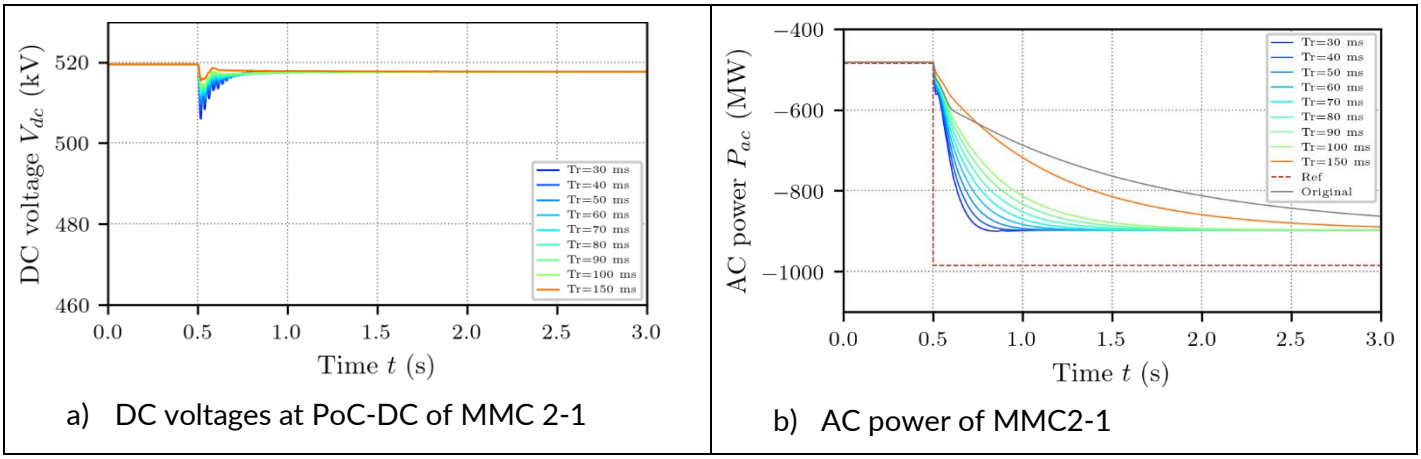
For $\zeta = 0.7$, it is known that the response time T_r is related to ω_n by,

$$T_r \approx \frac{3}{\omega_n}$$

With this relation, T_r is defined as the time that the DC voltage enters the ± 5 % band around the DC voltage reference in case of a step reference change. From the above expressions, the PI controller gains for a given T_r can be uniquely determined.

The same simulations as in the previous section were performed using the above equations, with the value of T_r varying from 30 to 150 ms. The obtained results are shown in Figure 76. In Figure 76a, the zoom of the voltage at PoC-DC of MMC 2-1 is shown. Figure 76b shows the active power response of MMC 2-1. As observed, the active power response of the DC voltage droop control significantly changes with the T_r, and hence the PI controller gains. The curve in gray, obtained using the same gain parameters as in the simulation in the previous section, indicates that the overall response time is well over 150 ms.

As the results show, the active power response characteristic under the droop control is greatly affected by the controller tuning. The controller tuning for Post Fault Active Power Recovery compliance is discussed in more detail in 0.

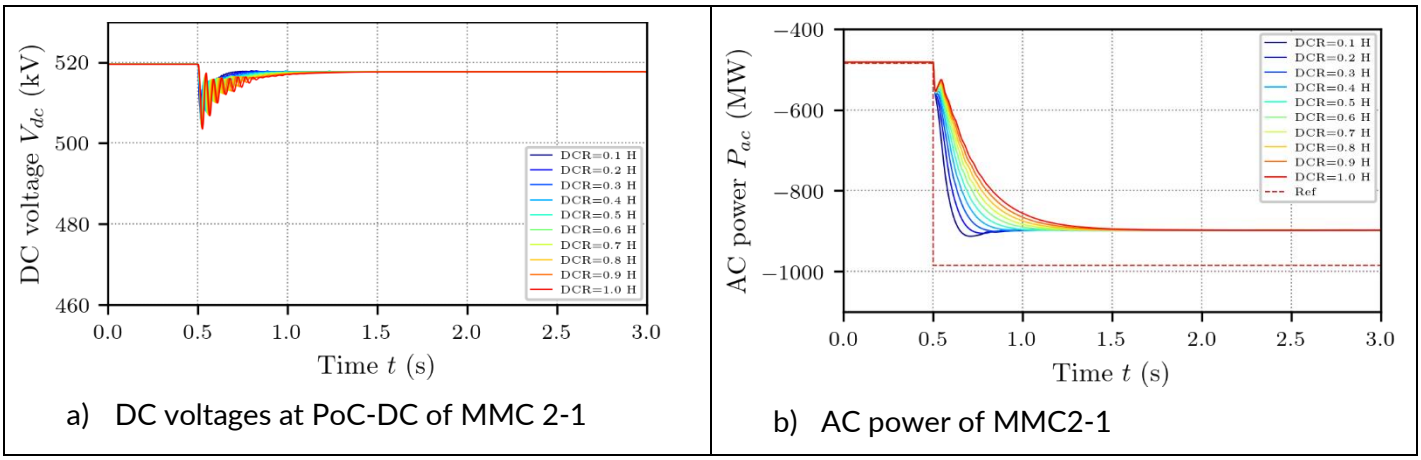


a) DC voltages at PoC-DC of MMC 2-1

b) AC power of MMC2-1

Figure 76 Simulation results: Coordinated change of set-point of active power in droop mode with varying T_r

The size of the DCR also affects this active power response. Therefore, fixing T_r at 30 ms, the same simulation was repeated with a varying size of the DCRs from 0.1 to 1 H. The results are shown in Figure 77. As seen in Figure 77b, the active power response becomes slower as the size of the inductance increases. This implies that, in order to achieve the desired active power response for a given DCR size, it is necessary to retuning the PI controller gains of the droop controller.



a) DC voltages at PoC-DC of MMC 2-1

b) AC power of MMC2-1

Figure 77 Simulation results: Coordinated change of set-point of active power in droop mode with Tr=40ms with varying DCR

6.3.3.2. Considerations on the steady-state deviation in active power

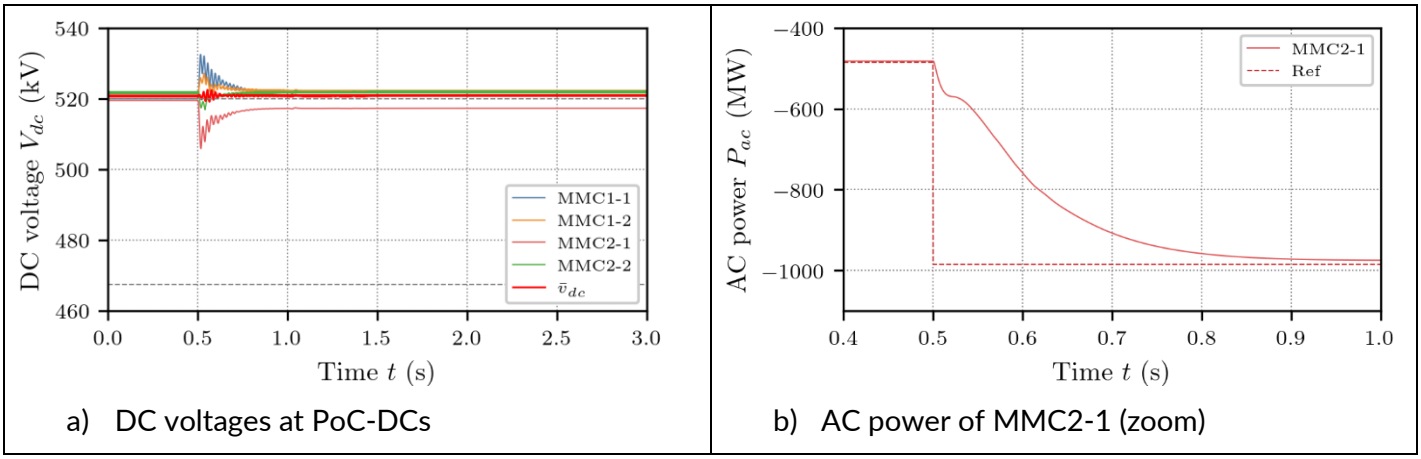
As seen in the previous simulations, when active power set-point was changed under droop control, steady-state deviation was observed. The deviation between the active power setpoint and the actual active power in steady state is caused by the fact that, unlike the frequency in AC system, the voltage at each node of the DC grid is different if a power flows through the nodes.

One of the possible solutions to this problem could be to use power flow algorithm to derive appropriate set-points of voltages and dispatch to all the stations at the same time as changing the power set-points. To demonstrate its feasibility, the same simulations was carried out with the setting indicated in Table 23. Besides, $T_r = 40$ ms and the size of DCR is 300 mH.

Table 23 Initial operational set-points for the studied case: Coordinated change of set-points of active power and DC voltage in droop mode

	Operating mode	Active power set-point P_{ac}^* [MW]	DC voltage set-point V_{dc}^* [kV]	Droop gain
MMC 1-1	Vdc droop control	-485 →+25	519.5 →522.2	0.05
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Vdc droop control	-485 →-985	519.5 →516.8	0.05
MMC 2-2	Fixed Ac power	+500	N/A	N/A

The obtained result is shown in Figure 78. As seen, the steady-state deviation is now eliminated completely. This further highlights the need of coordination by the DC grid controller.



a) DC voltages at PoC-DCs

b) AC power of MMC2-1 (zoom)

Figure 78 Simulation results: Coordinated change of set-point of active power and DC voltages in droop mode

It is important to note that dynamically changing the DC voltage set-points and active power setpoints is challenging for conventional control methods. Calculating, solving the power flow algorithm, and dispatching to each station in such a short timeframe without causing stability problems due to communication delays is complex and requires proper control.

6.3.4. Empirical understanding on the dynamic over- and under-voltages in MTDC grid under droop control

While the steady-state voltage profile in the DC grid is predominantly determined by the assigned droop gains, the dynamic behavior of the grid in case of disturbance, especially dynamic over and under voltages, is determined by control parameters.

In order to identify factors that influence the dynamic behavior of the system, the voltage dynamic in case of converter blocking was analyzed using the detailed simulation model of Use case 1.1. The scenario considered here is a sudden blocking of offshore station MMC1-2 at t=0.5s, resulting in a loss of 500 MW of power injection. The size of DCR was varied from 300, 600, and 900mH, and T_r value from 30, 50, 100, 200ms. The results are shown in Figure 79 and Figure 80. Note that the voltages were measured at the busbar, i.e. beyond the DCR seen form the MMC.

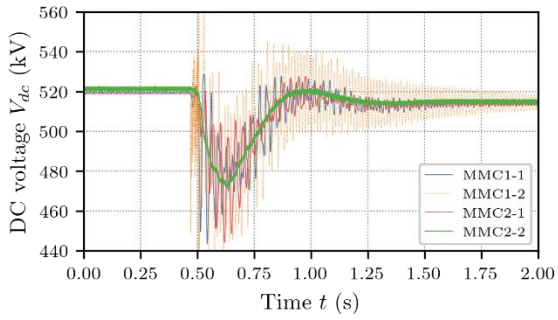
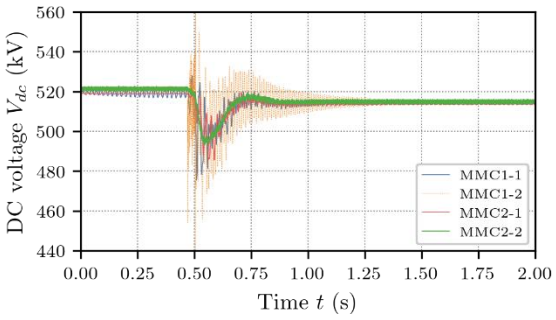
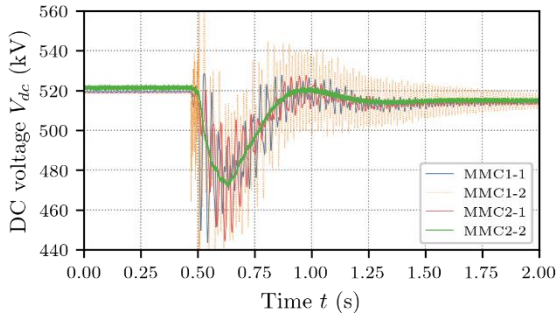
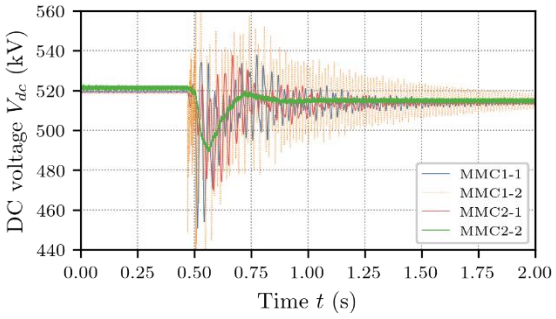
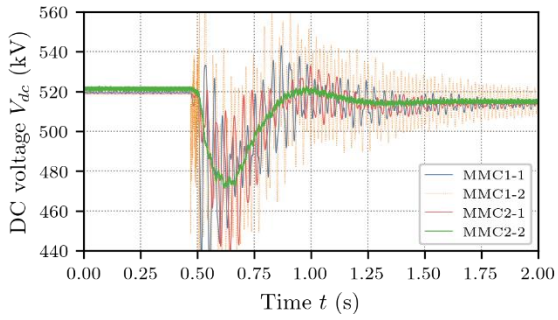
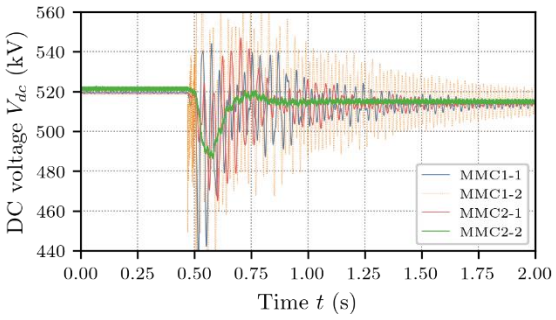
DCR size\Tr	200ms	100ms
300mH		
600mH		
900mH		

Figure 79 Simulation results of detailed use case 1.1 mode: Droop=0.05

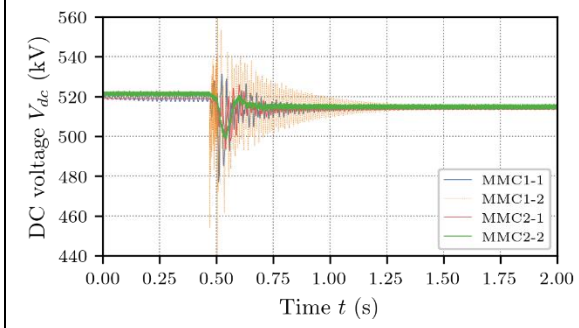
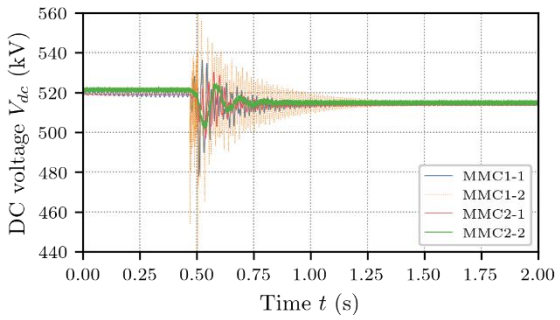
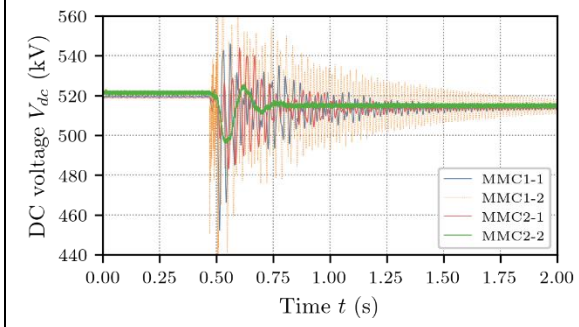
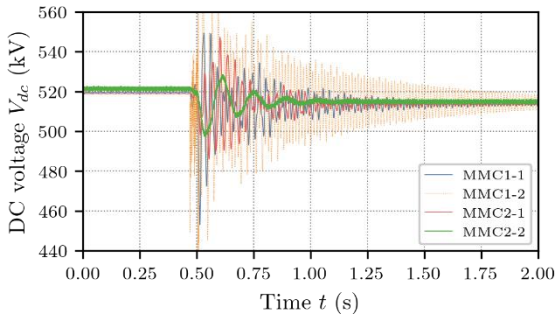
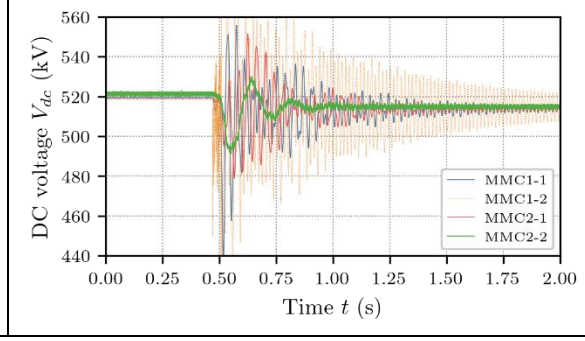
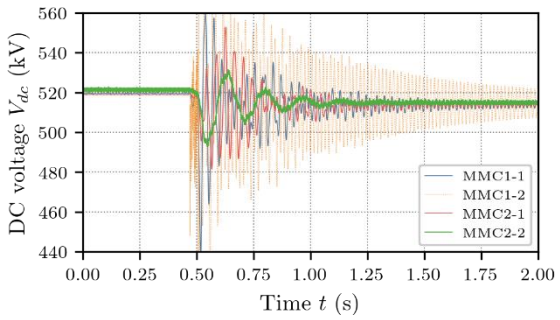
DCR size\Tr	50ms	30ms
300mH		
600mH		
900mH		

Figure 80 Simulation results of detailed use case 1.1 mode: Droop=0.05

From the observation, the dynamics of the DC voltages in case of a large power disturbance (i.e. in this case a sudden power deficit due to the blocking of an MMC injecting power) are characterized by three main components: a common DC voltage mode, a steady-state deviation determined by the droop gain, and fast oscillating components excited by the blocking of offshore station MMC1-2.

High-frequency oscillating components of 30~100 Hz can be observed, and they showed a clear increasing of oscillation peak trend with respect to the increase of DCR value. These components may depend on the choice of droop scheme and can be resolved by an appropriate filter design as proposed in [24]. However, this requires identification of the frequency components of the entire system by a small-signal analysis considering the DCR size and an appropriate filter design, which is deemed outside the scope of this project.

On the other hand, an interesting trend is observed for common DC voltage mode, which is well represented in the voltage of MMC 2-2. While the common DC voltage mode shows a clear dependence on the T_r value, the impact of the DCR size is not significant.

6.3.5. Methodology for specifying the dynamic over- and under- DC voltage requirements

The dependence on the dynamic DC voltage behavior of the system under droop control on the value of T_r and the little influence of the DCR size, confirmed in the previous section, indicate the possibility of estimating the dynamic voltage profile by a simplification that reproduces the influence of T_r.

Therefore, by extending the transfer function analysis on the fixed DC voltage control mode verified in Section 6.2.2, the following describes a simplistic methodology to reproduce the dynamic characteristics of the voltage under the primary DC voltage control.

Taking advantage of the similarity with a fixed DC voltage controller with the selected droop control scheme, a simplified block diagram representation of the system under the droop control is proposed as shown in Figure 81. Assuming that all droop-controlled stations are implemented with the same scheme, they are aggregated and represented by the factor N_{droop}, which corresponds to the number of the available droop-controlled stations.

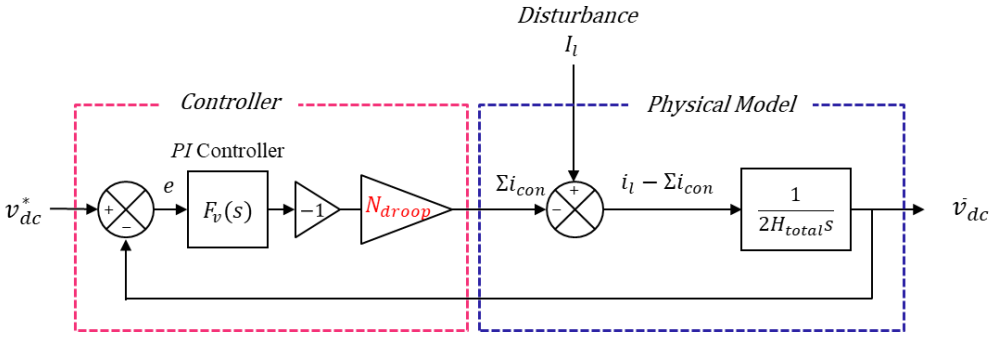


Figure 81 Simplified closed-loop model of typical HVDC system under primary DC voltage control

Through the same procedure presented in 6.2.2, the response of the voltage error against step disturbance in the time domain is given by

$$e(t) = L^{-1}\left\{TF(s) * \frac{I_{dis}}{s}\right\} = \frac{I_{dis}}{2H_{total}\omega_n} e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}}$$

where

$$\omega_n = \frac{3}{T_r}\sqrt{\frac{H_{mmc}N_{droop}}{H_{total}}}, \qquad \zeta = 0.7\sqrt{\frac{H_{mmc}N_{droop}}{H_{total}}}$$

And the estimated peak voltage V_{peak} is given by

$$e_{peak} = e(t_{peak}) = \frac{I_{dis}}{2H_{total}\omega_n} e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\tan^{-1}\frac{\sqrt{1-\zeta^2}}{\zeta}}$$

$$V_{peak} = V_{dc,0} + e_{peak}.$$

To confirm the validity of the derived formulas and assumptions, a comparison with simulations was performed. Using the same detailed model of use case 1.1, with two onshore AC/DC converter stations in droop mode (i.e., $N_{droop} = 2$), a blocking of MMC 1-2 (worst-scenario of 1GW loss of injection) is imposed at t=0.5s. The results obtained for two different droop gains (0.05 and 0.10) are shown in Figure 82. The estimated peak value and timing are plotted in red and black dashed lines, respectively. The estimated results compared to simulations

show some underestimation. This is because the steady-state voltage deviation due to the droop control is not considered in the derived formula. Therefore, the estimated values considering the steady-state voltage deviation prediction shown in 6.3.1.1 as an offset are shown in the blue lines. As observed, the peak value of the DC voltage falls within the estimated peak value added with a steady-state offset component.

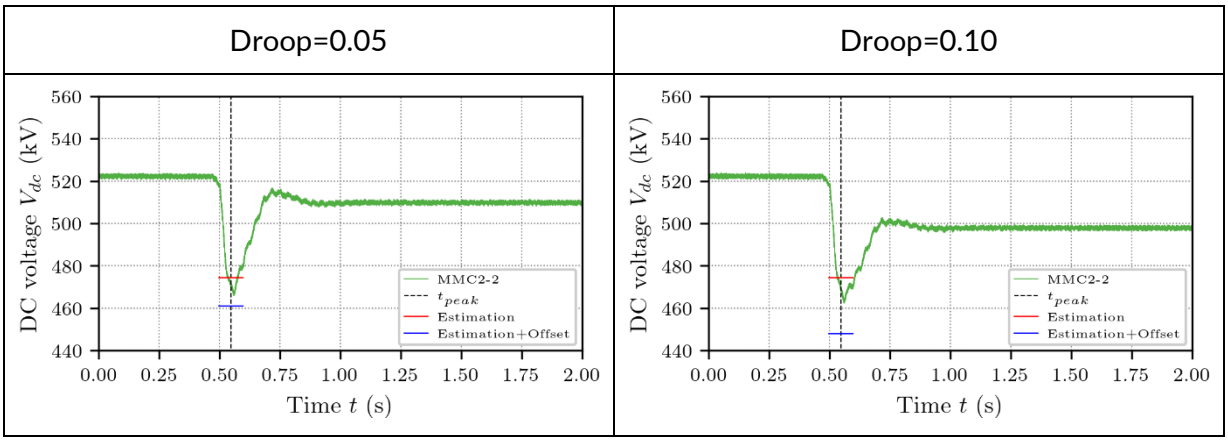


Figure 82 Validation of the derived analytical formulas of the peak dynamic DC voltage by comparison with dynamic peaks obtained from PSCAD simulations on detailed Use case 1.1

To verify the generality of the proposed method, validations were performed on the larger grids use case 1.2 and use case 2. A blocking of MMC 4-2 (loss of 500 MW of injection) was considered as the test scenario. The DCR size was set to 300 mH, and the droop controllers are all set to T_r=100ms.

The obtained results are shown in Figure 83. Some variation in DC voltage is observed among the stations. However, the derived formulas are still able to estimate peak voltages with sufficient accuracy.

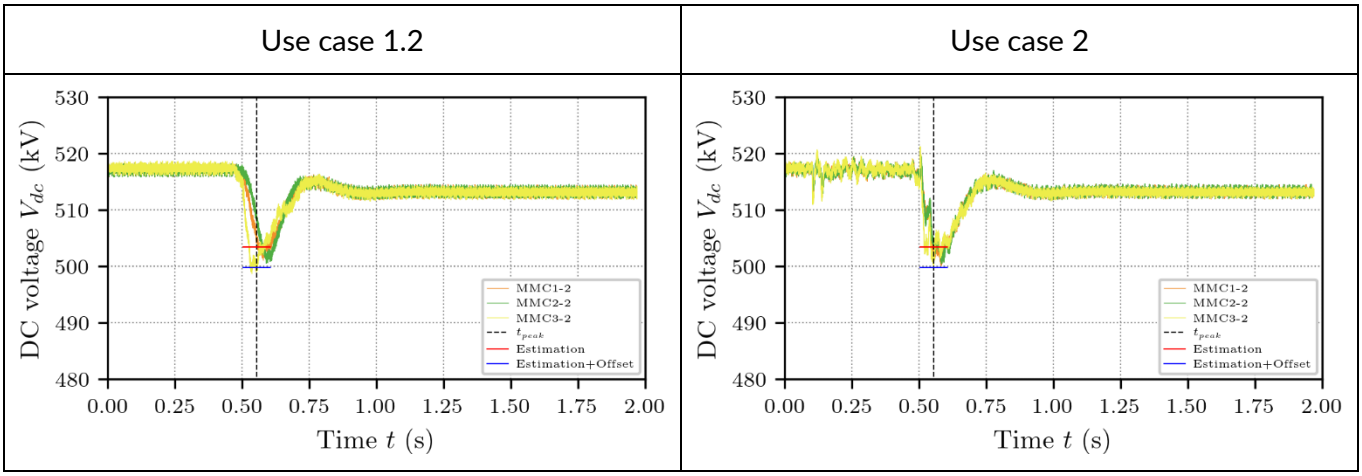


Figure 83 Validation of the derived formulas of the peak dynamic DC voltage by comparison with simulations using use case 1.2 and 2

It was shown that the proposed simplistic approach can capture the global behavior of the system, taking the number of the stations and the assigned droop parameters as inputs. However, for detailed parameter tuning considering all the modes of the system, a MIMO approach is recommended.

6.3.6. FR and PR definition

Table 24 Functional requirements related to primary DC voltage control

ID	Functional requirement
General 23	The AC/DC converter should be capable of activating DC voltage droop mode. When operating in DC voltage droop mode, the converter should be capable of responding DC voltage deviation in the connected DC network by adjusting active power (or DC power or DC current) in accordance with the specified parameters for the DC voltage droop mode.

Table 25 Parameters related to primary DC voltage control for disturbance management

ID	Symbol	Characteristic/Events	Range	Comments
37	sP_UDC	defines the change of active power reference in response to a deviation of the DC voltage from its reference value sP_UDC = (ΔUDC/UDCnom) / (ΔP/Pn), A droop constant could be individually defined for each voltage section.	$[0.00 - 0.10]$	The droop gains should be determined taking into account the credible contingencies that can occur in the given grid topology and acceptable post-contingence DC voltage deviation in average.
38	sIDC_UDC	defines the change of DC current reference in response to a deviation of the DC voltage from its reference value. sIDC_UDC = (ΔUDC /UDCnom) / (ΔIDC/IDCnom). A droop constant could be individually defined for each voltage section.	$[0.00 - 0.10]$	

Controllability requirement

To eliminate inconsistencies in behavior between the stations, The response times of the DC voltage in the DC voltage droop control mode should be verified by consistent rules and verified as proposed for the fixed DC voltage control in 6.2.1.

Table 26 Parameters related to DC voltage droop control mode

ID	Symbol	Characteristic/Events	Range	Comments
139	Ts	time required for the DC voltage droop controller to settle to a new reference value after sudden changes, typically defined for a precision within 5% absolute distance to new reference value	$[30 - 120]$ ms	

Active power controllability requirement

In addition to the dynamic response requirement in fixed active power mode, the active power dynamic response in DC voltage droop mode should be specified.

It was observed that the dynamic response of the active power depends on the size of the DCRs in the grid. Therefore, this must be verified considering the size of the DCRs.

A change in the active power set-point within an MTDC inevitably involves a change in the power of other converters as well as a change in the power flow within the grid. This should be taken into account in the definition of the requirements for converters.

Table 27 Parameters related to fixed active power control mode

ID	Symbol	Characteristic/Events	Range	Comments
138	Ts	time required for fixed active power control mode to settle to a new reference value after sudden changes	$[100 - 200]$ ms	

6.4. Post Fault Active Power Recovery

The Post Fault Active Power Recovery (PFAPR) requirement is stipulated in 6.15 of the Dutch NetCode Elektriciteit: Dutch National HVDC Grid Code (Sept 2022), which specifies particular requirements as:

The HVDC system is capable of active power recovery as soon as possible after a fault in the AC network:

- → the active power recovery begins at an AC voltage level of 90% of the pre-fault voltage;
- → the maximum allowed time for active power recovery is 0.2 s unless otherwise agreed because of technological limitations or transmission system security;
- → the magnitude of active power to be restored is at least 90% of the pre-fault active power;
- → the tolerance of the recovered active power is 10% of the pre-fault active power;

In this section, the essential factors that affects the compliance to the PFAPR specification are demonstrated.

6.4.1. Empirical understanding on the dynamic over- and under-voltages in droop controlled MTDC grid

The studied case for demonstration is depicted in Figure 84. MMC 2-1 is used as the subject of the verification. The set-points of the AC/DC converter stations are summarized in Table 28. The DCR size is set to 300 mH, and the droop controllers are tuned to have T_r=100ms.

To reproduce the worst-case situation, this demonstration assumes that the active power transfer capability is initially set to zero just before PFAPR starts. At t_{ev}=0.25s, active power is forced to zero and the reactive power injection is initiated. Assuming the duration of the incident is 500ms, at t=0.75s, the active power transfer capability is restored.

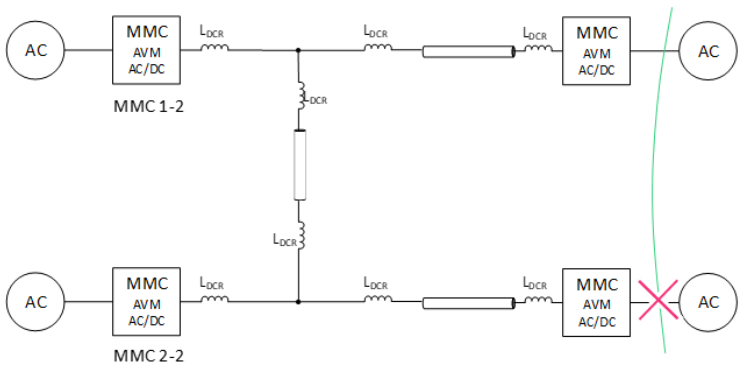
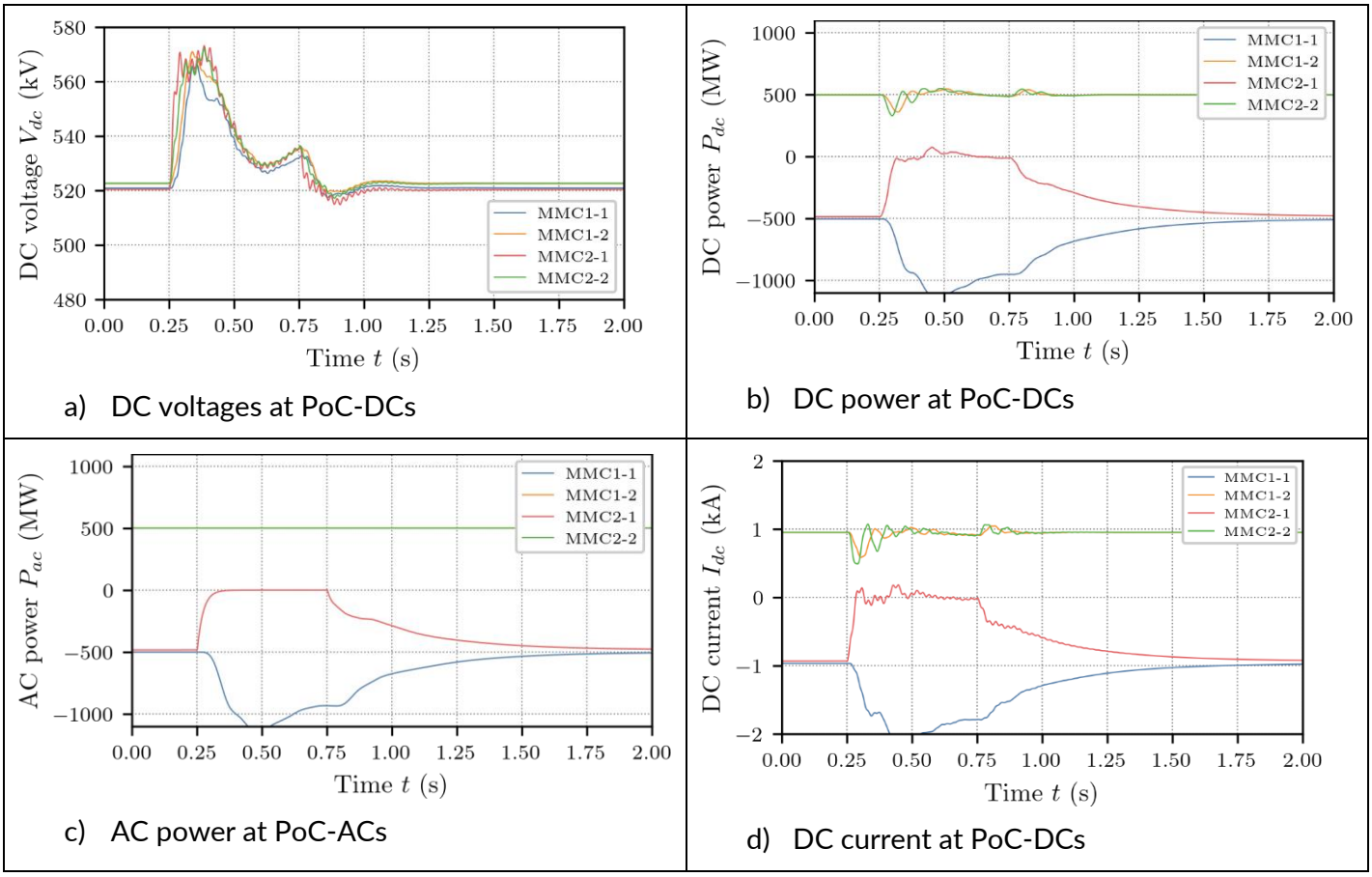


Figure 84 Study case (use case 1.1)

Table 28 Initial operational set-points

	Operating mode	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Droop gain
MMC 1-1	Vdc droop control	-485	519.5	0.05
MMC 1-2	Fixed AC power	+500	N/A	N/A
MMC 2-1	Vdc droop control	-485	519.5	0.05
MMC 2-2	Fixed Ac power	+500	N/A	N/A

The obtained results are shown in Figure 85. In Figure 85a. the DC grid voltages are depicted. If the active power transfer capacity of the converter stations in the grid changes, or in this case, when the active power evacuation by the onshore stations decreases, the grid will encounter an excess of energy, which will cause the DC voltages to increase. This increase is contained by the primary DC voltage control discussed in the previous section. Notable here is the behavior of the DC voltages after t=0.5s, i.e. after the initiation of the PFAPR. As observed, the DC voltages find the same steady state before the incident without any external intervention. This is because the DC voltage profile is uniquely determined for a given power profile, and, unless the assigned control parameters or the grid configuration changes, PFAPR works to restore the entire system to its initial condition naturally.



a) DC voltages at PoC-DCs

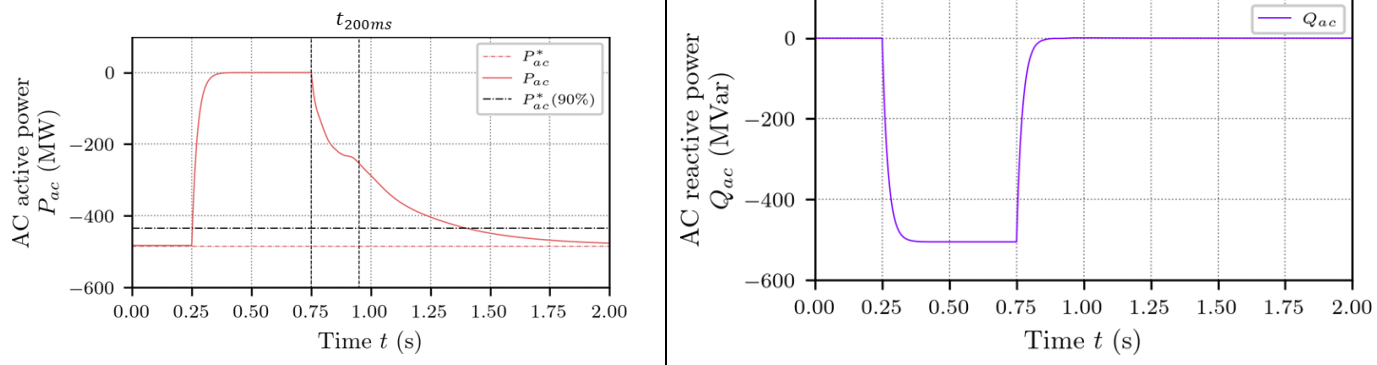
b) DC power at PoC-DCs

c) AC power at PoC-ACs

d) DC current at PoC-DCs

Figure 85 Simulation results: Demonstration of PFAPR

In Figure 86, the zoom of the active and reactive power of MMC 2-1 is shown. The vertical line with the mention of t_{200ms} indicates the time constraint of 200 ms after the AC grid voltages recovery. The PFAPR requirements specify to recover 90% of the pre-fault active power with 10% tolerance. The horizontal dash-dot line indicates the 90% level of the pre-fault active power, to which the active power is expected to be recovered before t_{200ms}. However, as seen, the PFAPR takes more than 500 ms and does not satisfy the specification.



a) AC active power at PoC-AC of MMC 2-1

b) AC reactive power at PoC-AC of MMC 2-1

Figure 86 Simulation results: Demonstration of PFAPR: Zoom on MMC 2-1

In order to identify the factors to be considered to comply with the PFAPR requirements, a sensitivity analysis was performed for DCR size (300, 600 and 900mH), T_r of the droop controller (30, 50, 100, and 300 ms), and the droop gain (0.05 and 0.10). Simulations were performed for each set of parameters. The PFAPR process is initiated at t=0.5s. The zoom of the active power of MMC 2-1 for droop=0.05 and 0.10 are shown in Figure 87 and Figure 88, respectively.

As a general trend, the influential factor on PFAPR compliance is the value of T_r of the droop controller. As shown in Section 6.3.4, the selection of T_r predominantly determines the dynamics of the whole system. Moreover, the active power control is controlled via the PI controller in the droop control scheme, so it is inevitably affected by the assigned value of T_r.

On the other hand, in all cases, the dynamic response becomes slightly slower as the size of the DCR increases. The impact of DCR can be said to be small compared to the influence of T_r, but still not negligible. Therefore, it is necessary to consider the size of the DCR in designing to meet the requirements of the PFAPR.

Finally, the selection of the droop gain also has a significant influence on the PFAPR performance. With respect to the value of droop, the larger the value of droop, the faster the speed of PFAPR. This is understandable because the change in the DC voltage reference value with respect to the deviation of the active power is proportional to the droop gain.

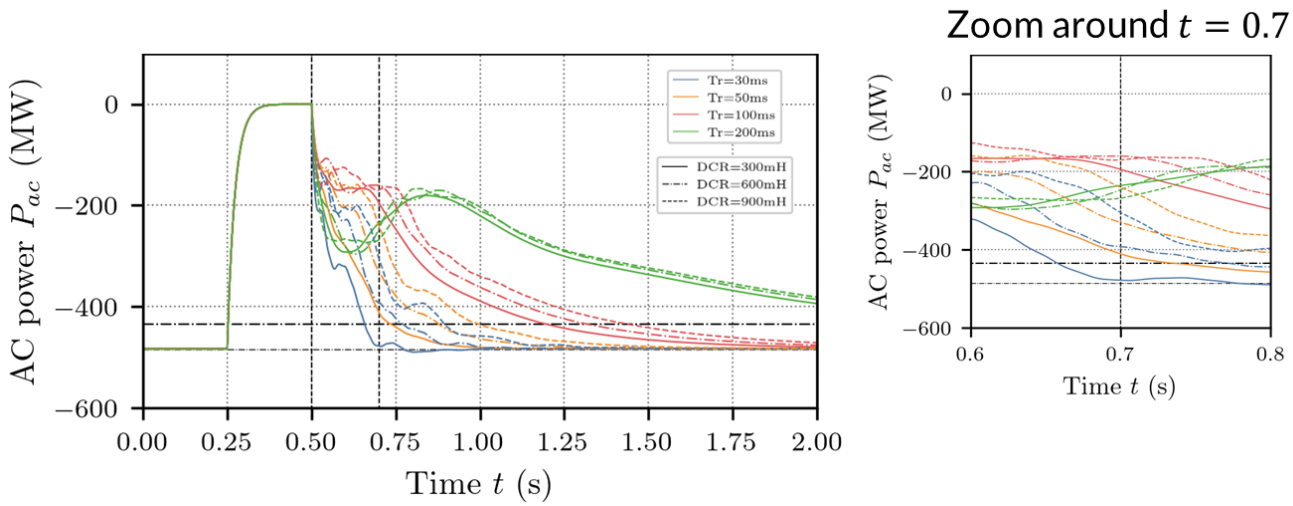


Figure 87 Sensitivity analysis results: PFAPR: Zoom on MMC 2-1 with droop=0.05 (the colors indicate the response time T_r, and the DCR size indicated by the line type, solid: -300mH, dash-dot: 600mH, dash: 900mH)

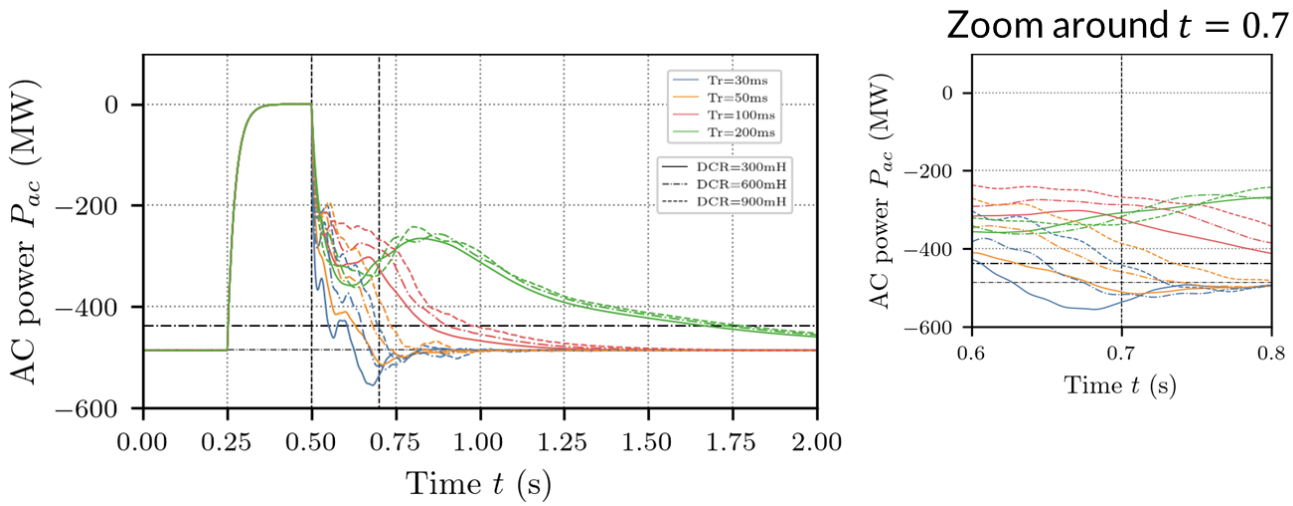


Figure 88 Sensitivity analysis results: PFAPR: Zoom on MMC 2-1 with droop=0.10 (the colors indicate the response time T_r, and the DCR size indicated by the line type, solid: -300mH, dash-dot: 600mH, dash: 900mH)

6.4.2. FR and PR definition

In this section, the impacting factors for the compliance of the PFAPR were analyzed. The dominant factors identified are the droop gain and the response time of the droop controller. Furthermore, the size of the DCR also has a non-negligible effect on the time to restore the pre-contingency active power. The correlation of each parameter is shown in Figure 89.

The current grid code allows a tolerance of 10% of the pre-failure active power, but for certain parameter sets, especially for large DCR sizes, the parameter ranges considered could not satisfy the required performance.

In this study, detailed investigation on the technical solutions inside the controller, such as the saturation mechanism of the inner controllers or the memory function of measurement values immediately after an

accident is not carried out. Therefore, the possibility of such technical solutions to achieve compliance even for parameter sets that could not comply in the studied case should be kept in perspective.

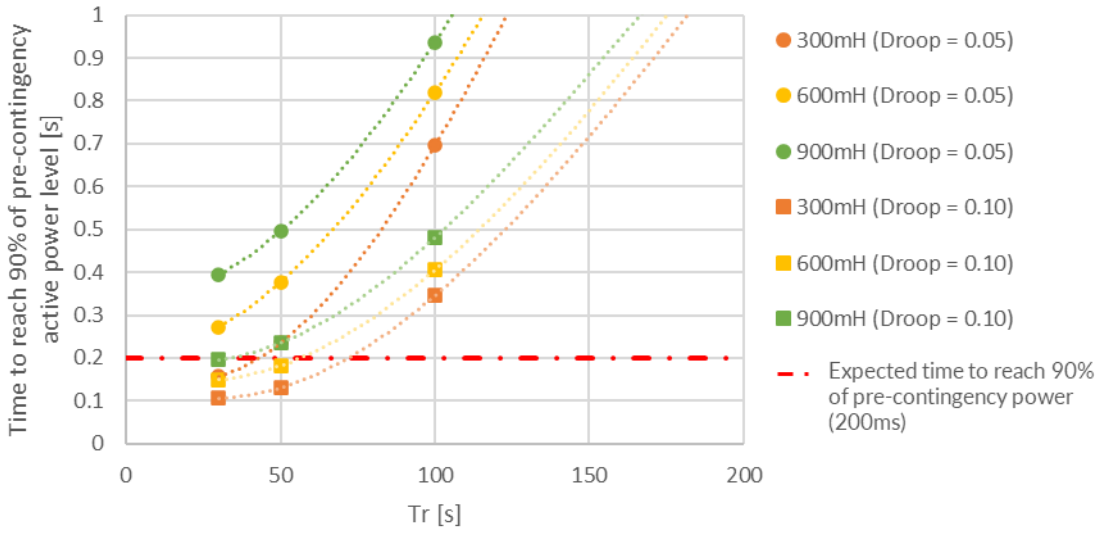


Figure 89 Summary of the sensitivity analysis results: PFAPR

Table 29 Functional requirements related to post-fault active power recovery

ID	Functional requirement
General 61	The relevant onshore TSO(s) must specify and agree on the time range, and the level of active power that shall be restored by the multi-terminal HVDC system during the post-AC fault period, in the affected AC network.

Table 30 Parameters related to primary DC voltage control for post-fault active power recovery

ID	Symbol	Characteristic/Events	Range	Comments
132	UAC_PFAPR	AC voltage level to initiate the active power recovery of the DC voltage	0.9 p.u.	unless otherwise agreed because of technological limitations or transmission system security
133	t_PFAPR	maximum allowed time for active power recovery	0.2 s	unless otherwise agreed because of technological limitations or transmission system security
134	%P_PFAPR	The magnitude of active power to be restored relative to the active power before the fault.	90 %	unless otherwise agreed because of technological limitations or transmission system security
135	ΔP_PFAPR	The tolerance of the recovered active power relative to the active power before the fault	10 %	unless otherwise agreed because of technological limitations or transmission system security

6.5. Secondary DC voltage control

This section discusses the need of the secondary DC voltage control and proposes a guideline for its specification. The primary DC voltage control takes immediate reaction to a sudden change in power balance to contain the DC voltage rise/drop and find a new equilibrium point different from the initial operating states. Therefore, although the post-contingency DC voltage remains within the acceptable range, the security margin of the DC voltage is reduced and may not be sufficient to cope with another contingency. For this reason, the secondary DC voltage control, in analogy to the secondary AC frequency control, is activated and brings back the voltage to the desired level and adjusts the power flow setpoints. In short, its main roles are threefold:

- Bringing back the voltage to the pre-contingency level
- Restoring the interchange power flow profile
- Free up the previously committed capacity for the primary DC voltage control

6.5.1. Empirical understanding on the secondary DC voltage control

To illustrate the role of the secondary DC voltage control, a demonstration by simulation has been carried out. The simulation was done using the developed STB of Use case 1.1, shown in Figure 91. The simulation scenario assumes following steps: at t=1s, the injection of the power from offshore station MMC 1-2 is dropped to zero. The resulting DC voltage drop is contained by the activation of the primary DC voltage, discussed in 6.3. Then, at t=5s, new set-points are dispatched to the onshore stations, i.e. MMC 1-1 and 2-1. Those new set-points are derived taking into account the actual wind generation, which is 500 MW. In Table 31, the summary of the transition of the set-points are provided.

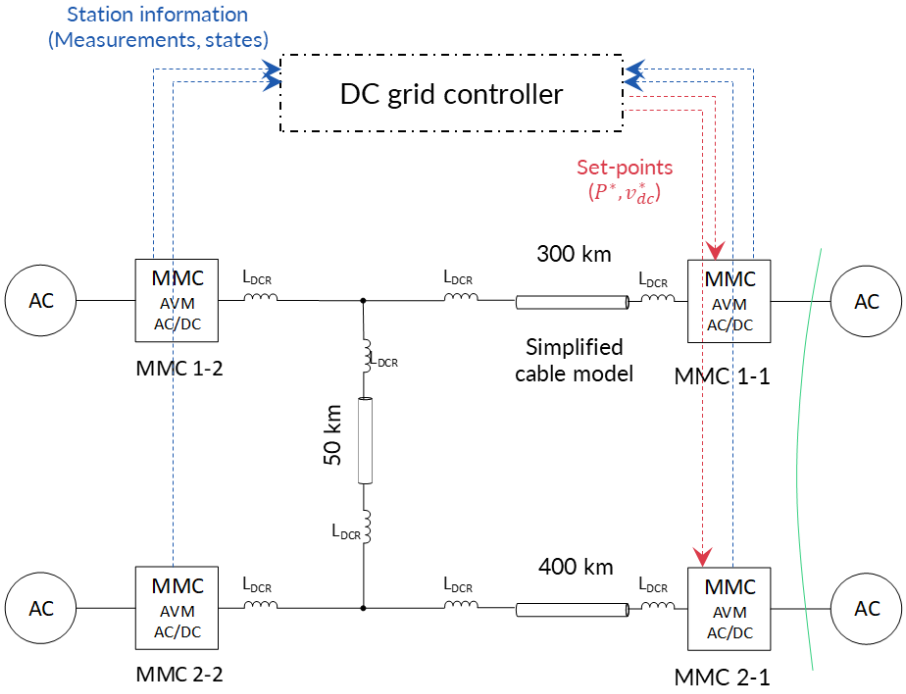


Figure 90 Simulation set-up for the demonstration of the secondary DC voltage control

Table 31 Operational set-points

	Operating mode	t<5s		t>5s	
		Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]	Active power set-point P_{ac}^{*} [MW]	DC voltage set-point V_{dc}^{*} [kV]
MMC 1-1	Vdc droop control	-485	519.5	-290	519.5
MMC 1-2	Fixed AC power	+500-> 0	N/A	0	N/A
MMC 2-1	Vdc droop control	-485	519.5	-205	519.5
MMC 2-2	Fixed Ac power	+500	N/A	+500	N/A

The obtained simulation results are given in Figure 91. Figure 91a shows the DC voltages. As seen, the sudden loss of power injection from MMC 1-2 resulted in a sharp drop of the DC voltage, which is successfully contained by the primary DC voltage control, and the system find the new equilibrium point, which is determined by the magnitude of disturbance (i.e. -500 MW) and the value of droop gain (0.05). At t=5s, assuming a dispatch from the DC grid controller, new set-points are assigned to the onshore stations. To demonstrate the flexible imbalance sharing by the secondary DC voltage control, different values are intentionally chosen for the two onshore stations. As observed, the voltages are recovered to the pre-contingency level. In Figure 92, the zoom of the active power of the onshore stations and their set-point values are shown. There is a difference from the setpoint up to t=5s. In other words, the primary DC voltage control reserves is consumed. However, after t=5s, the actual power set-point and the new setpoint matches. This means that the reserves have been successfully released.

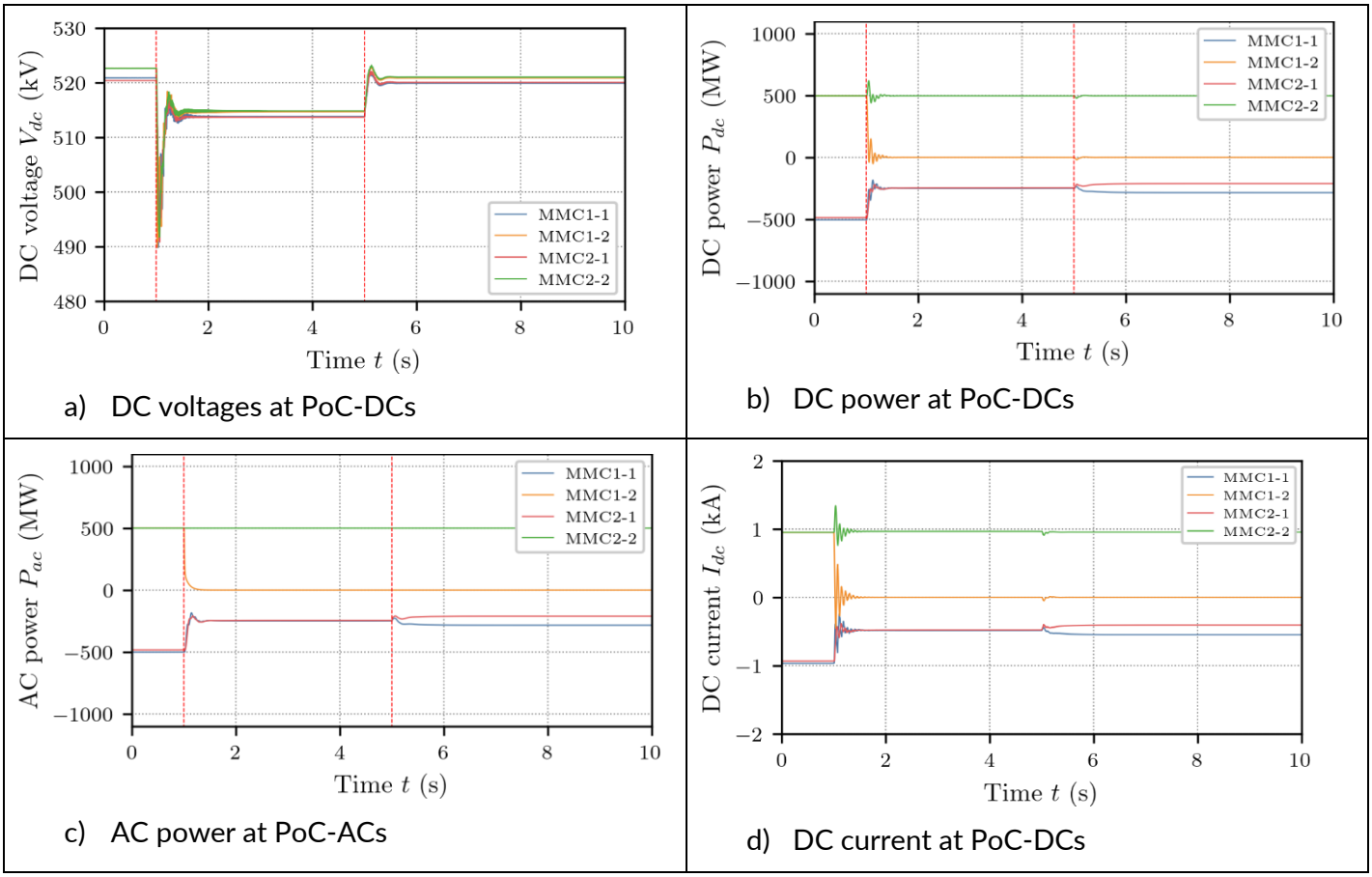


Figure 91 Simulation results of secondary DC voltage control

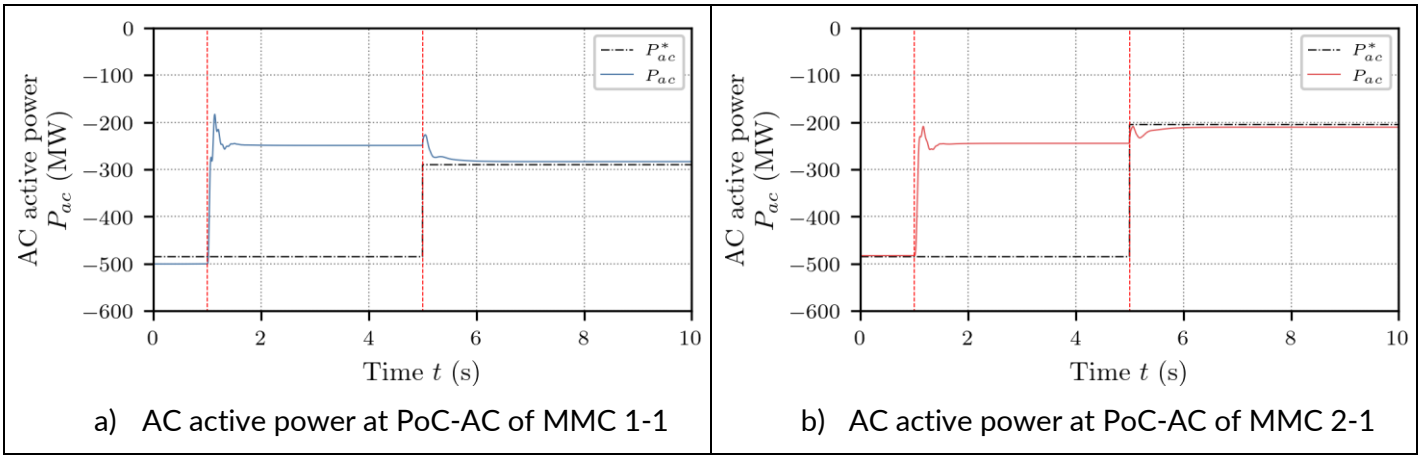


Figure 92 Simulation results of secondary DC voltage control: Zoom on active power of MMC 1-1 and 2-1

6.5.2. FR and PR definition

In this section, the principle of operation of secondary DC voltage control was demonstrated. In the event of an unscheduled event, new setpoints must be calculated, dispatched, and achieved based on accurate assessment of the situational grid state.

In the demonstration presented in this section, the new setpoints were dispatched to each station as step signals, but as can be found in the definition of the converter schedule in the CENELEC report, each setpoint should be dispatched together with associated ramp speed from the DC grid controller in practice.

As the name implies, the specifications required for secondary DC voltage control would follow the frequency restoration process (secondary AC frequency control). Since secondary AC frequency control is typically initiated after the required full activation time of primary AC frequency control, the initiation of secondary DC voltage control should also be after the subordinate control actions, e.g., primary DC voltage control or DBS activation, are achieved. The order of ~10s proposed by CENELEC is deemed reasonable for secure accomplishment of the secondary DC voltage control.

On the other hand, the completion of secondary DC voltage control should be sufficiently faster in order to avoid unnecessary FRR activations by the secondary AC frequency control of the connected AC systems. It is desirable that secondary DC voltage control satisfy these requirements while minimizing the risk from communication delays and malfunction by appropriate ramp speeds.

Table 32 Functional requirements related to secondary DC voltage control

ID	Functional requirement
Master_Control3	The DC grid controller should be capable of sending set points and commands to: the AC/DC grid controller: operational signals, at least the following: -final converter schedule -Station information -Alarm signals the converter stations: operational signals, at least the following: -Converter schedule including the required parameters for ancillary services -Autonomous adaptation control rules -Signals related open-loop control command -Signals related to DC grid protection, if any -Alarm signals the DC switching station. -Signals related open-loop control command -Signals related to DC grid protection, if any -Alarm signals
Master_Control7	The DC grid controller should be capable of reacting to unscheduled events resulting in deviations from the scheduled power flow by modifying the converter schedule according to the predefined rules and specified cycle time

Table 33 Parameters related to secondary DC voltage control

ID	Symbol	Characteristic/Events	Range
2	t_sec_DC_ini	time for initiation of the secondary DC volage control	[1-10] s
3	t_sec_DC_comp	time for completion of the secondary DC volage control	[10-30] s

6.6. Conclusions

→ Using Graph theory, a STB has been proposed to estimate the steady state DC voltage whatever the DC grid size. The STB has been validated against use case 1.1, use case 1.2 and use case 2.

→ For fixed DC voltage control mode, two factors have been identified which impact the DC voltage stability: the response time of DC voltage controller and DCR size. For each combination of these two factors, the proposed methodology based on STB allows to estimate the damping ratio and natural frequency of the system. Hence, it is possible to select the DCR value and response time that satisfy the damping ratio limit. For example, with a response time of PI controller of 50 ms the DCR should be less than 600 mH to respect a damping ratio limit of 10%.

→ For droop DC voltage control, using the selected droop scheme, the impact of droop gain, DCR value and the response time of PI controller have been analyzed for controllability and disturbance management. The results show that the steady state voltage profile is predominantly determined by the assigned droop gains where the dynamic behavior in case of disturbance is mainly determined by response time with little influence of the DCR size. An STB based on analytical formula has been proposed which allows to estimate the peak voltage in case of disturbance. The validation against use case 1.1 and use case 2 show that the derived formulas is able to estimate the peak voltages with sufficient accuracy.

→ For Post Fault Active Power Recovery, the sensitivity analysis results show that the droop gain, the DCR value and the response time have an important impact. According to the required time to reach 90% of pre-contingency active power level, some combinations of these three factors will not be acceptable. For example, in case of 300 mH for DCR with 5% of droop gain, the response time of PI controller shall be less than 40 ms to satisfy the requirement of 200 ms for PFAPR.

→ For the Secondary DC voltage control, the objectives and the needs for this control were demonstrated through simulations using a system consisting of the developed AVM model. Relevant parameters necessary for this control were also proposed.

7. Functional group - DC Protection

7.1. AC system constraints - temporary and permanent stop of active power

7.1.1. Methodology

CENELEC standards introduce the concept of temporary and permanent stop of active and reactive power after a DC grid contingency. However, no values are provided for the amount of temporary and permanent power loss, nor for the duration of the temporary stop. From the AC grid perspective, it should be ensured that no DC grid contingency should endanger the AC grid stability. More generally, the impact of DC grid contingency on the AC grid should be minimized. The most critical impact of a DC contingency on the AC grid is deemed to be the frequency stability, i.e. the frequency deviation that may result from a loss of active power transmitted by the DC grid. The considered AC grid stability limits are reminded in Table 34.

Table 34: AC grid stability constraints

Indicator	**Value**	**Source**
Reference incident	-3 GW	ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance
Minimum Instantaneous Frequency after Loss of Generation (Nadir).	800 mHz	ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance
Maximum RoCoF	1Hz/s	Frequency Stability Evaluation Criteria for the Synchronous Zone of Continental Europe

A DC grid contingency will impact those indicators differently:

- The temporary loss of DC power should be less than the reference incident for the CE synchronous zone, i.e. a loss of 3GW. In addition, the instantaneous loss of power will induce a RoCoF that should be less than 1 Hz/s.
- The nadir will depend on the size of the power imbalance as well as on its duration.
- In case of a permanent loss, the lost active power should eventually be compensated for using Frequency Restoration Reserve (FRR). Thus, the maximum permanent loss of active power should correspond to the level of FRR, which depends on the country considered. It was in addition considered that, for very low probability events as defined in [5], the FRR can be shared between countries and can go up to 2 GW.

The requirements for active power loss after DC fault are listed in Table 35.

Table 35: Temporary and permanent stop requirements after a DC fault in relation to AC side constraints

Requirement	Parameter	Comment
Temporary stop power	3 GW	Dimensioning event at CE level, from ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance
Temporary stop duration	To be determined	Such that frequency deviation is limited to 800 mHz.
Permanent stop power	[0.7 ; 1 ; 1.4] GW	Corresponds to FRR level, per country (DK: 0.7GW, NL: 1 GW, DE: 1.4 GW)
Permanent stop power (low probability event)	2 GW	Considering FRR can be shared for such events

The adequate temporary stop duration to avoid a frequency deviation above 800 mHz will be determined using a simplified representation of AC grid inertial response.

7.1.2. STB: Simplified AC side inertial response

A simplified AC side inertial model is developed using transfer functions based on

- A single machine equivalent model of a synchronous area that represents the variation of frequency Δf after a power imbalance ΔP

$$\frac{\Delta f}{\Delta P} = \frac{f_n}{S_n(2H\,s + k f_n)},$$

where $f_n = 50$ Hz is the nominal frequency, H is the total inertia of the system (in s), S_n is the total load of the system (in GW), and k represents the self-regulating effects of some loads.

- A simplified Frequency Containment Reserve (FCR) profile that represents the power injected by the FCR after a variation in frequency Δf

$$\Delta P_{FCR} = \exp(-\tau_d s)\frac{G}{1+\tau s}\Delta f,$$

where τ_d represents an activation delay, τ the time constant of the FCR activation, and G the power frequency characteristic of primary frequency control. In addition, the power output of the FCR is limited to ± 3 GW.

The chosen parameters are provided in Table 36.

Table 36: Main tuning parameters for AC inertial response model

Parameter	**Value**	**Comment**
Self-regulation of load k	1%	ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance
Minimum network power frequency control	15 GW/Hz	ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance
FCR delay τ_d	1s	
FCR time constant τ	4s	Based on 50% response in 15s, from ENTSO-E P1 Policy 1 - Load-Frequency Control and Performance

Examples of two inertial response are provided in Figure 93 where a temporary loss of 3GW during 4s with a permanent loss of 2GW is compared with a case where no DC recovery occurs (i.e. the loss of 3GW is permanent). Two sets of system parameters have been derived from TYNDP 2050 scenario corresponding to low inertial situations (top: H = 1.65 s, Sn = 311 GW; bottom: H = 0.8 s, Sn = 312 GW).

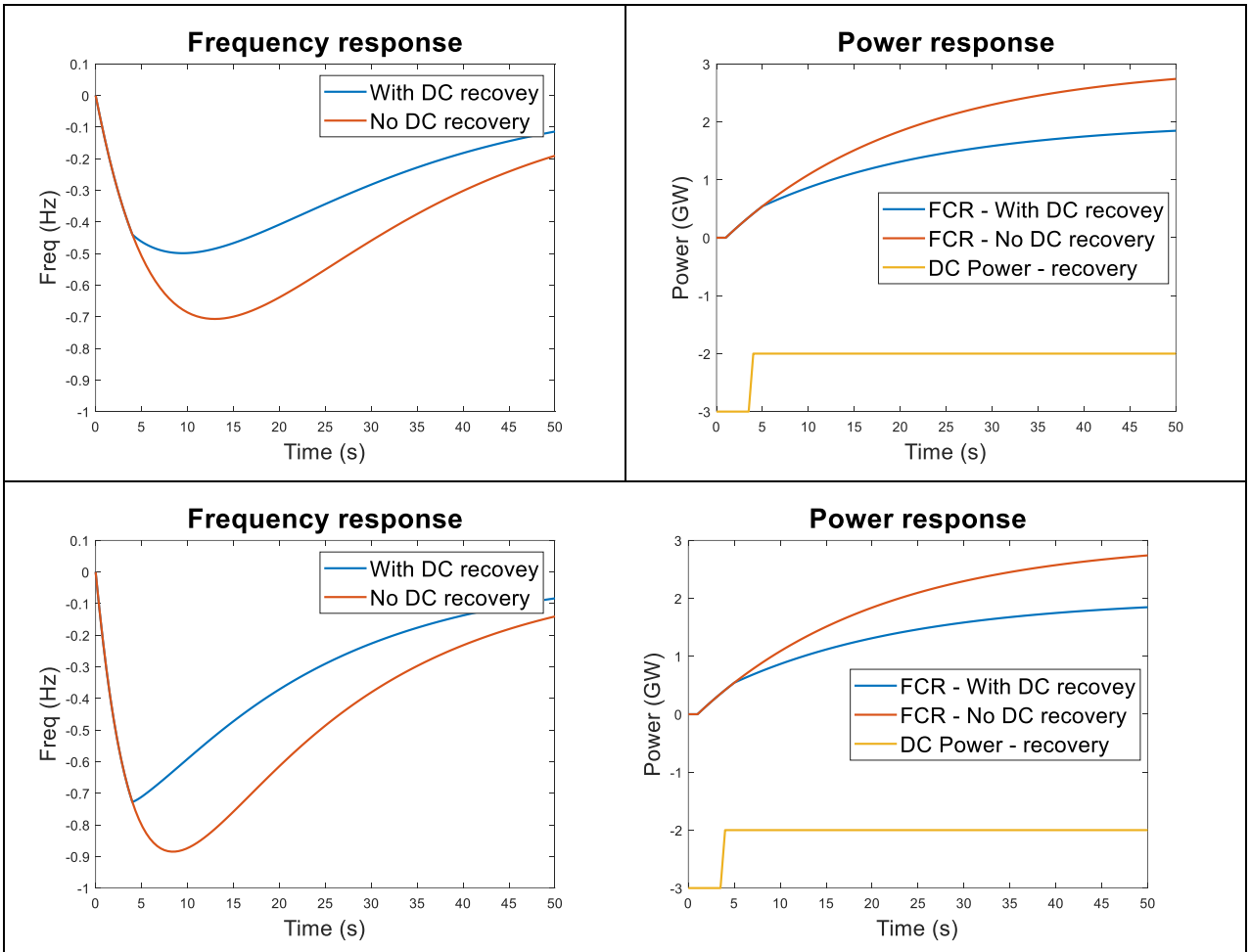


Figure 93: Frequency and power inertial response for two low inertia scenarios (top: H = 1.65, Sn = 311 GW; bottom: H = 0.8s, Sn = 312 GW). The considered event is temporary loss of 3 GW and a permanent loss of 2 GW. Case with a DC power recovery in 4s is compared with a case without DC recovery.

7.1.3. Results for dimensioning test scenario

Determining the impact of DC contingency on the AC grid requires the knowledge of the future inertia and load of the system. Several scenarios considering the future European power system have been listed in Table 37. The first two scenarios come from internal computations, based on TYNDP trajectories.

Table 37: Future inertia and load of European power system according to different scenarios

	Inertia (s)	**Load (GW)**	**Kinetic Energy (GWs)**	**Source**
Scenario 1 (2050)	1.65	311	516	Internal, TYNDP based
Scenario 2 (2050)	0.8	312	250	Internal, TYNDP based
High load (2030)	6	450	2700	ENTSO-E, Inertia and Rate of Change of Frequency (RoCoF)
Low load (2030)	6	200	1200	
High RES (2030)	3	450	1350	
TYNDP 2040	1.25	600	750	

The dimensioning scenario will combine a low inertia and a low load. For comparison, however, a fixed “worst case” load of 200 GW was considered. The effect of different inertia and temporary stop duration is evaluated for two different events:

- A temporary stop of 2 GW with a permanent stop of 1 GW (the system is able to recover 1 GW out of the 2 that are lost). This corresponds to a rather representative fault event (e.g., offshore converter fault).
- A temporary stop of 3 GW with a permanent stop of 2 GW (the system is able to recover 1 GW out of the 3 that are lost). This corresponds to the worst case considering the maximum temporary and permanent loss, without consideration on the type of event that can induce such a loss.

The maximum frequency deviation for those two cases is given in Figure 94. Key observations are:

- The critical RoCoF value of 1Hz/s is never reached in none of the scenario. This somehow excludes the need for synthetic inertia to maintain RoCoF above an acceptable limit. This also suggests that the limit of 3GW for the temporary loss could be released, at the cost of a harder requirement on the nadir (e.g., faster recovery).
- Generally, DC power recovery in the order of 5 to 10s can limit the nadir and hence improve AC grid security. For DC recovery occurring after 10 to 15s, the nadir is not affected as the DC recovery occurs after the nadir has been reached (indicated by straight lines). Note, however, that in such situations a partial recovery of DC power would still limit the use of the FCR.
- For a typical event (first case: 2 GW temporary stop, 1 GW permanent stop), the 800 mHz limit is never reached, even in the low inertia cases and without considering DC power recovery.
- For a critical event (second case: 3 GW temporary stop, 2 GW permanent stop), the frequency deviation will exceed 800 mHz in the low inertia situations if the DC recovery is not fast enough. Assuming inertia

level below 1s (for a load of 200 GW) are unrealistic, a **requirement of 4s for the power recovery appears appropriate.**

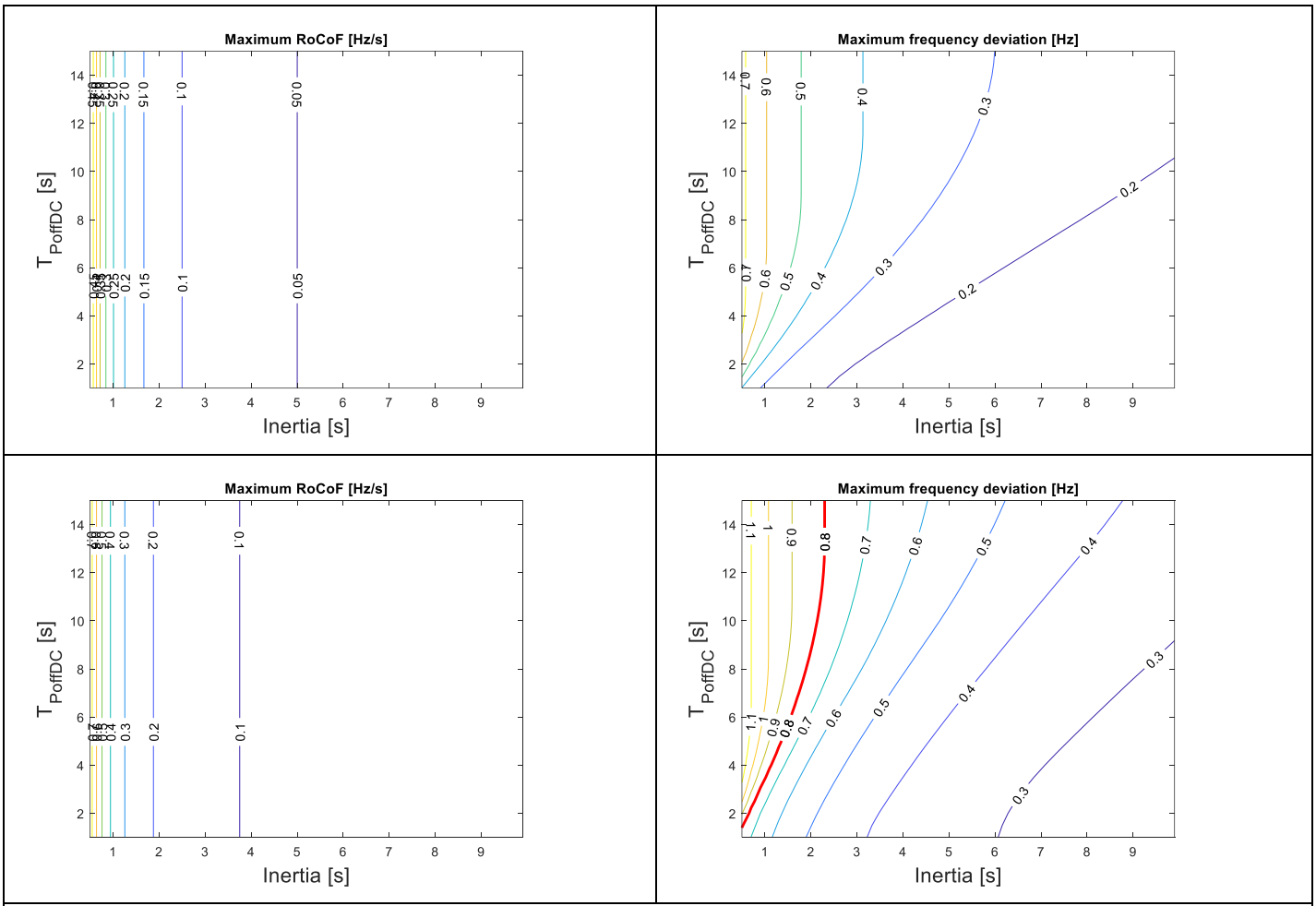


Figure 94: Maximum RoCoF (left) and maximum frequency deviation (right) for various inertia and temporary stop duration. The system load is 200 GW. The event is a temporary loss of 2 GW and permanent loss of 1 GW (top) and a temporary loss of 3 GW and temporary loss of 2 GW (bottom).

7.1.4. Conclusion

As shown in this section, the acceptable level and the duration of temporary and permanent stops for the HVDC grid depend on multiple factors, in particular the considered system (inertia, load…) as well as the considered events. Assuming a fixed limit on the maximum temporary loss of active power that corresponds to the dimensioning incident of 3GW, a temporary stop duration of 4s allows to limit the frequency deviation within the 800mHz limit for system with inertia as low as 1.1s. The requirements for temporary and permanent stop are summarized in Table 38. If, however, instead of considering a loss of 3GW constraint, the constraint on a

maximum RoCoF of 1Hz/s is imposed, the acceptable temporary loss of power could increase up to 4GW when assuming a shorter DC restoration time of about 2s is possible to limit the nadir to 49.2 Hz.

Table 38: Requirements for temporary and permanent stop of active power after HVDC event, considering AC stability constraints

Requirement	Parameter	Comment
Temporary stop power	3 GW	Dimensioning event
Temporary stop duration	4s	Such that nadir > 49.2 Hz
Permanent stop power (high probability event)[6]	[0.7 ; 1 ; 1.4] GW	FRR per country
Permanent stop power (low and very low probability event)	2 GW	Shared FRR

Following the NSWPH use configurations, the case where the MTDC is connected to a single synchronous zone was investigated. In the case where the DC grid interconnects several AC zones, the definition of the TS and PS stop could be done with at least two different approaches:

- → The approach presented here can be performed for each connected AC zone, and a single TS and PS stop requirement can be applied to the entire DC grid, according to the most restrictive AC zone conditions. In this approach, a weak AC zone would impose harsh constraints to the entire DC grid.
- → A TS and PS can also be defined for each connected AC zone, depending on each synchronous area characteristic. The maximum power loss could for instance be different for the different zones, leading to different constraints on the protection design.

Based on the new proposed AC system requirements, the calculation of the amount of loss of power[7] during PS and TS for an HVDC building block considering the different type of faults is shown in appendix 12.1.

[6] Failure rates:

Failure rates for different type of faults as proposed in [32]:

Type of fault	Failure rate*
Line fault	**3.5** f/100y/100km
Active fault on a DC breaker	**1.5** f/100y
Busbar fault	**0.74** f/100y/bay
Line fault + DC breaker failure	**2*10^{-4}** occ/100y/100km
Spurious Trip	**1.4** occ/100y
Sympathetic Trip	**1*10^{-4}** occ/100y/100km
Busbar fault + DC breaker failure	**1*10^{-4}** occ/100y
Converter failure	**3** occ/1y

(*) y=year; f=failure; occ=occurrence

[7] The detailed methodology for the calculation of the amount of loss of active power during PS and TS can be found in section 5.4.2 of [32].

7.2. Converter blocking specification

In MTDC grids, all converters contribute to the control of either DC voltage or active power or a combination of both (droop control). A converter blocking implies that the control is disabled, and the capacitors are bypassed. It further introduces a power imbalance. An uncontrolled blocking of multiple converters, for example due to overcurrent protection during DC faults, has important consequences on the voltage and power restoration as fewer converters can provide support. In the context of this study, it is assumed that automatic deblocking during the restoration process is not a functionality of the converter, and thus a blocked converter is considered as not operational during the restoration process. In this context, it is of utmost importance that the blocking criteria of the converters in an MTDC grid are aligned with the protection strategy. To ensure this, a functional requirement on DC current blocking constraint is proposed in the following section.

7.2.1. Overcurrent protection

In Point-to-Point (PtP) links, the main objective of blocking is to protect the IGBT modules from overcurrent, which is related to their technical limits. Hence, the blocking criterion is chosen by the manufacturer and is usually based on overcurrent identification in converter arms. However, other criteria such as submodule overvoltage or undervoltage protection or combinations of current increase and overcurrent are possible to protect the sub-modules of the MMC converter and ensure its controllability. Furthermore, measurement delays and security margins must be chosen to anticipate the blocking before the technical limits are reached. This is for now subject to the manufacturer which implies that for a given technical limit of IGBT current, the blocking trip order can be sent out at a different time according to the principle and the delays that are used by the manufacturer. This results in a zone of uncertainty as shown in Figure 95 by the 'blocking area depending on manufacturer blocking criteria'. As mentioned above, the objective in MTDC grids is not only to protect the IGBT modules but also to guarantee the protection sequences and grid restoration for multiple fault scenarios. The acceptable number of blocked MMCs is strictly limited in order to respect the maximum loss of infeed.

As a conclusion, the converter blocking criteria in MTDC grids must be specified at the DC-PoC based on the DC current. Therefore, in the following, a functional requirement on the blocking criteria based on the DC current $i_{dc,blk}$ is proposed[8]. It is understood that the DC blocking criteria must consider both the technical limits of the converter and the protection design in the DC grid. Figure 96 gives an illustrative overview on blocking criteria requirements in PtP links compared to MTDC grids.

[8] From our point of view, the DC current blocking criteria is the criterion that allows systematic DC protection design based on DC grid entities. Indeed, the converter arm currents are influenced by other factors on the DC side (i.e. DC reactor size) but also aspects on the AC side (short-circuit ratio, offshore or onshore connection, phase angle, load flow). For these reasons, the DC current blocking criterion is the preferred option.

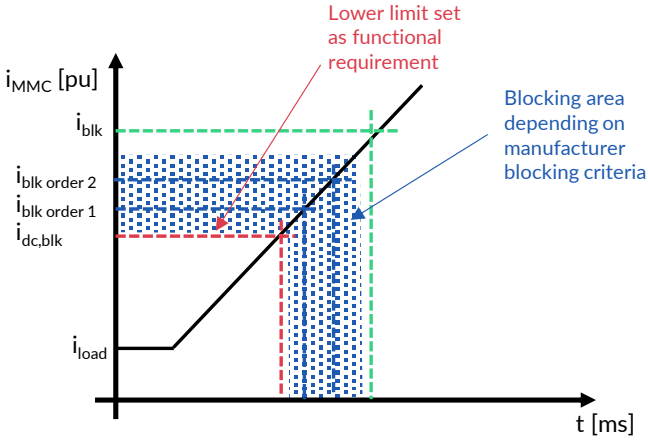


Figure 95 DC blocking criteria illustration

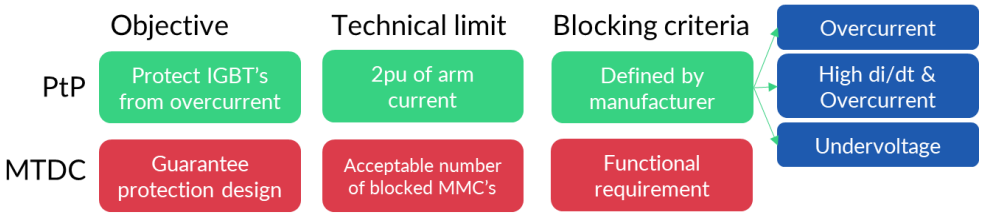


Figure 96 Synthesis of blocking criteria requirements in PtP links and MTDC grids

Arm currents are linked with DC current i_{dc} and AC current i_{ac} by the following equation:

$$i_{arm} = \frac{i_{ac}}{2} + \frac{i_{dc}}{3}$$

Rated arm current and rated DC current are defined by the following equations[9]:

$$i_{arm,r} = \frac{P_r}{2\sqrt{3}V_{ac,r}} + \frac{P_r}{3V_{dc,r}}, i_{dc,r} = \frac{P_r}{V_{dc,r}}$$

When linking arm current blocking constraints and DC current blocking constraints, it becomes clear that it also depends on the evolution of the AC current (see Figure 100) and hence on the AC grid characteristics such as short-circuit ratio which can be significantly different on the onshore or the offshore side.

[9] In this study: $i_{arm,r}$=2kA, $i_{dc,r}$=1,905kA

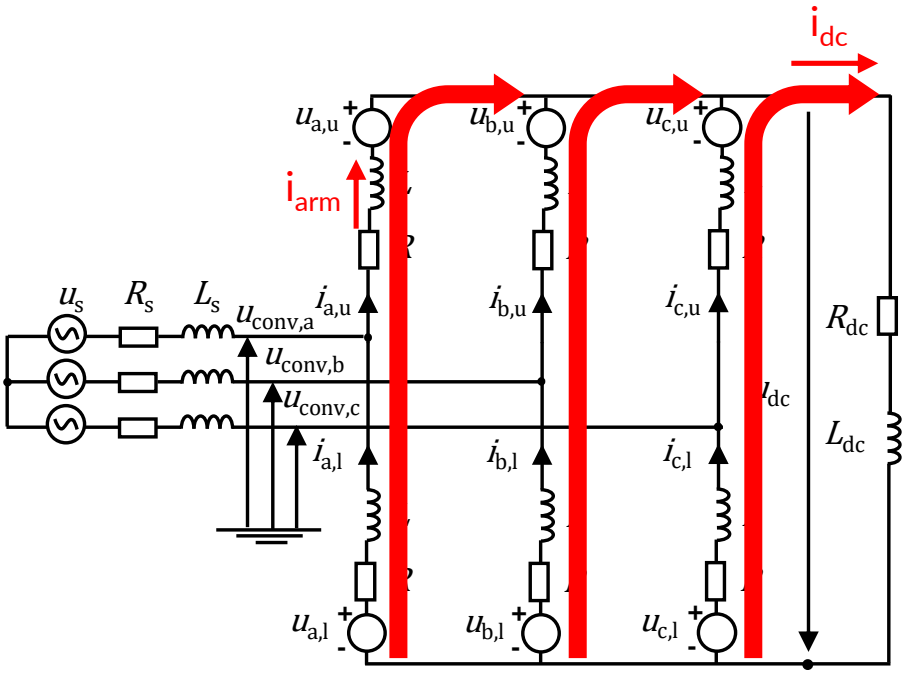


Figure 97 Illustration of submodule capacitor discharge during DC faults; relation between DC current, arm currents and AC currents

The AC current evolution is further dependent on the DC reactors. In fact, a low value of DC reactor leads to a fast increase of current in case of a fault such that submodule discharge of the converter is limited and AC current cannot change as fast in amplitude. If $\Delta i_{ac} \approx 0$, then there is a direct link between the arm current and the DC current $\Delta i_{arm} = \frac{\Delta i_{dc}}{3}$. However, in case of a high DC reactor, the increase of i_{dc} is rather slow, submodule capacitors discharge significantly and hence the AC current amplitude increases. Another important factor is the type of converter control and the control parameters. In the following, the dependency between secondary AC currents, arm currents and DC currents will be investigated. It should be noted that the goal is to show some trends depending on the aforementioned influencing factors.

The test circuit is an MMC connected to a Thevenin voltage source with an equivalent short circuit power of 24GVA (base case). On its DC side, the MMC is connected to a current source which imposes a DC load flow via a DC reactor (see Figure 98). The MMC is controlled in DC voltage control mode.

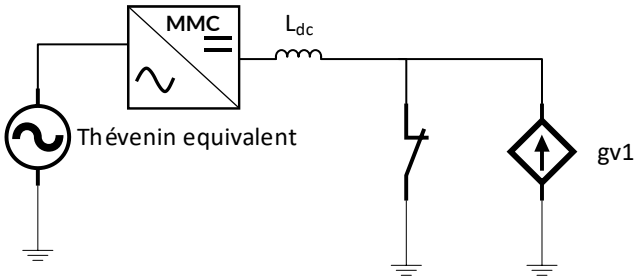


Figure 98 Test circuit for arm current and DC current comparison

7.2.1.1. Influence of DC reactor

Figure 99 gives an illustrative overview on the evolution of the DC currents, arm currents and secondary AC currents during faults for low DC reactor values (left) and high DC reactor values (right). In this example, a DC current blocking constraint of $i_{dc,blk}$=9.525kA=5pu is chosen (note that the nominal DC current is $i_{dc,r}$ = 1905 A). The pre-fault load flow is 1pu and the fault is applied at 0.01s. First, it is obvious that the DC reactor value influences significantly the time from fault inception to MMC blocking as it limits the rise of DC fault current: 1.1ms for 50mH and 17.9ms for 1000mH. In the case of 50mH, the AC current on the secondary side does not show any visible changes until blocking. This implies that the rise of arm currents is essentially depending on the capacitor discharge and hence on the rise of the DC current. In the case of 1000mH, the amplitude of the secondary AC currents increases from 3.2kA before the fault to 5kA at the instant of blocking. This example shows that the increase of arm currents depends on both DC side and AC side quantities. It should be noted that the DC reactor is one influencing factor among others such as: pre-fault load flow, AC grid short-circuit ratio, DC current blocking constraint, MMC control parameters and MMC energy level.

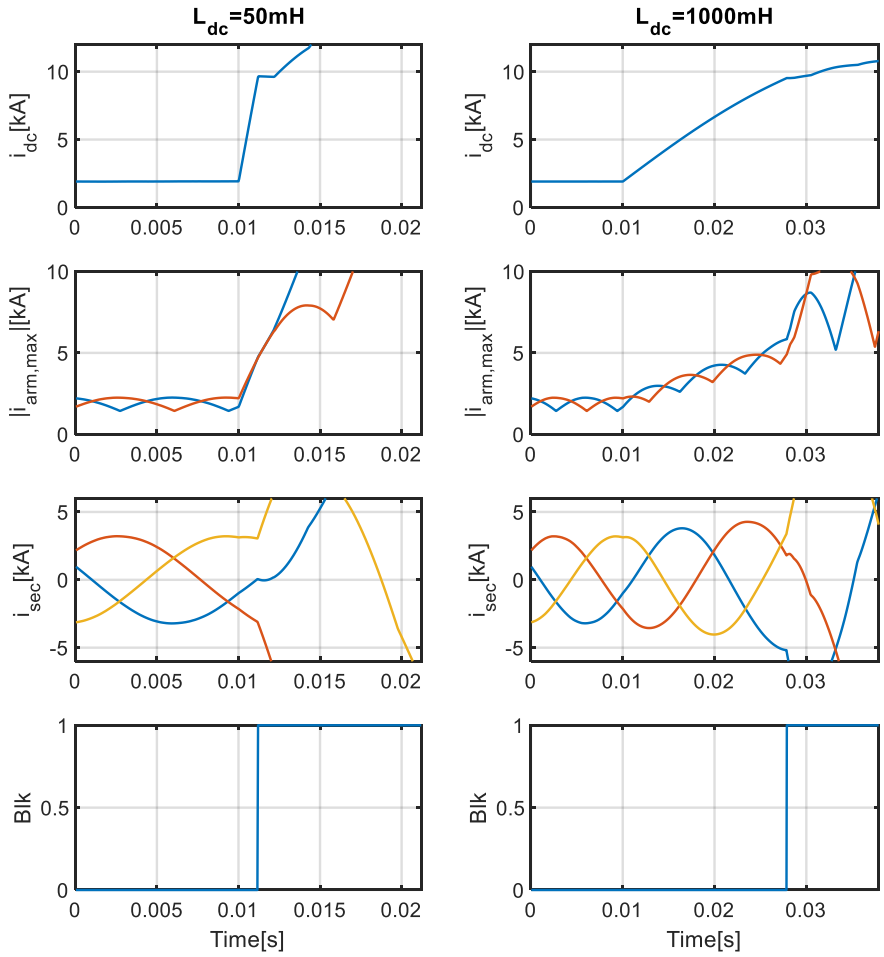


Figure 99 Evolution of MMC DC current, maximum of lower (red) and upper (blue) arm currents, secondary AC currents and MMC blocking signal ($i_{dc,blk}$=9.525kA/5pu); left: low DC inductor value (50mH), right: high DC inductor value; Short-circuit power: 24GVA

7.2.1.2. Influence of short-circuit ratio

The impact of the strength of the AC grid is investigated in this section by varying the short-circuit ratio of the Thevenin equivalent voltage source. A weak grid (10GVA) and a strong grid (43GVA) are compared. The results of the sensitivity analysis are shown in Figure 100. It can be concluded that the strength of the AC grid has very little impact on the maximum arm currents for a given DC current blocking criterion, when comparing AC grids with short circuit power higher than 10GVA. It should be noted that for purely converter-based grids, such as offshore configurations, another investigation would be required considering the upper short-circuit current limit of wind farms.

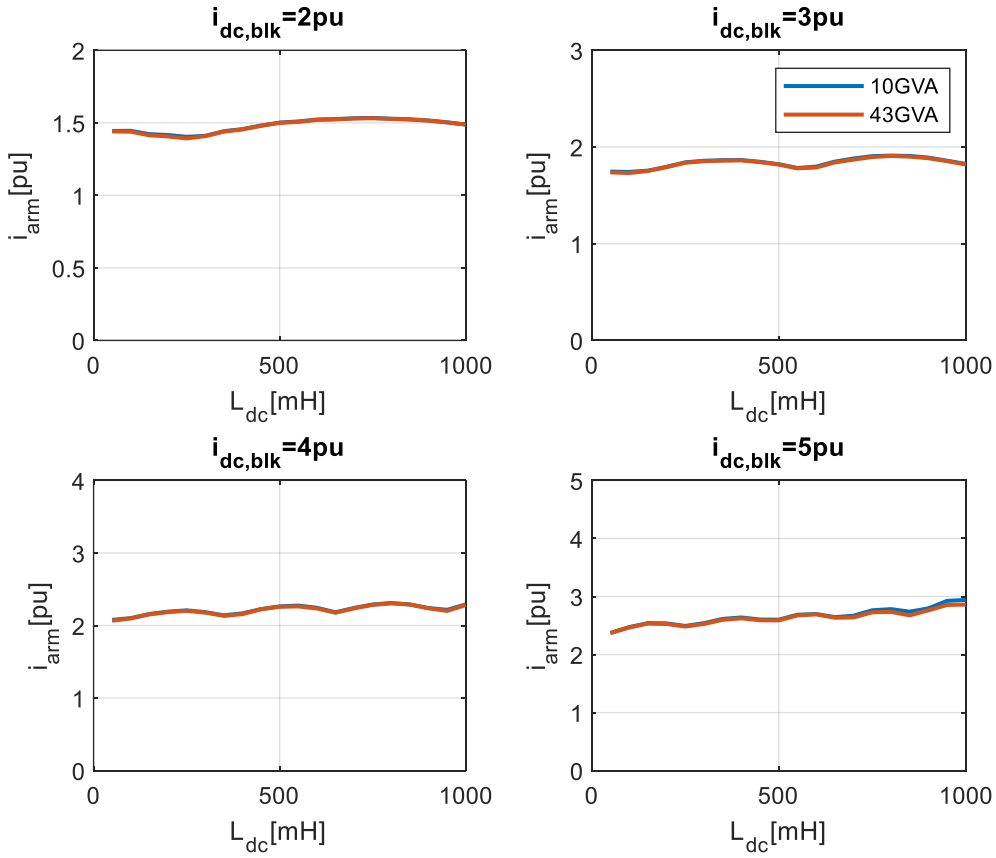


Figure 100 Sensitivity analysis of maximum arm currents[10] for different DC current blocking constraints and different short-circuit ratios; Converter response time T_r=100ms

[10] For the determination of the maximum arm current all arm currents from fault inception to reaching of DC current blocking limit are observed and the maximum value is retained for each simulation.

7.2.1.3. Influence of pre-fault load flow

In this section, the influence of pre-fault load flow on arm current increase will be investigated. Figure 101 shows the results for three different load flow scenarios. The dashed vertical line indicates the moment of blocking. The fault is applied at 0.01s. The following observation can be made:

→ The initial di/dt of the DC fault current is identical. Obviously, the margin between pre-fault DC current and DC current blocking limit is higher for a rated negative load flow (6pu) and lower for a rated positive load flow (4pu). This implies that the time to block is lower for positive load flow.

→ The absolute values of the arm currents are not equal at the moment of blocking. Hence, the AC currents have an impact on the maximum arm currents.

→ Phase and amplitude of AC currents do not change for the case of P_{LF}=1pu. In fact, the converter cannot change the power reference as it is already at maximum value. However, for P_{LF}=-1pu and P_{LF}=0pu, the converter reacts to the voltage drop at the DC side by injecting power. Hence, the phase angle and the amplitude of AC currents change. This has an impact on the arm currents.

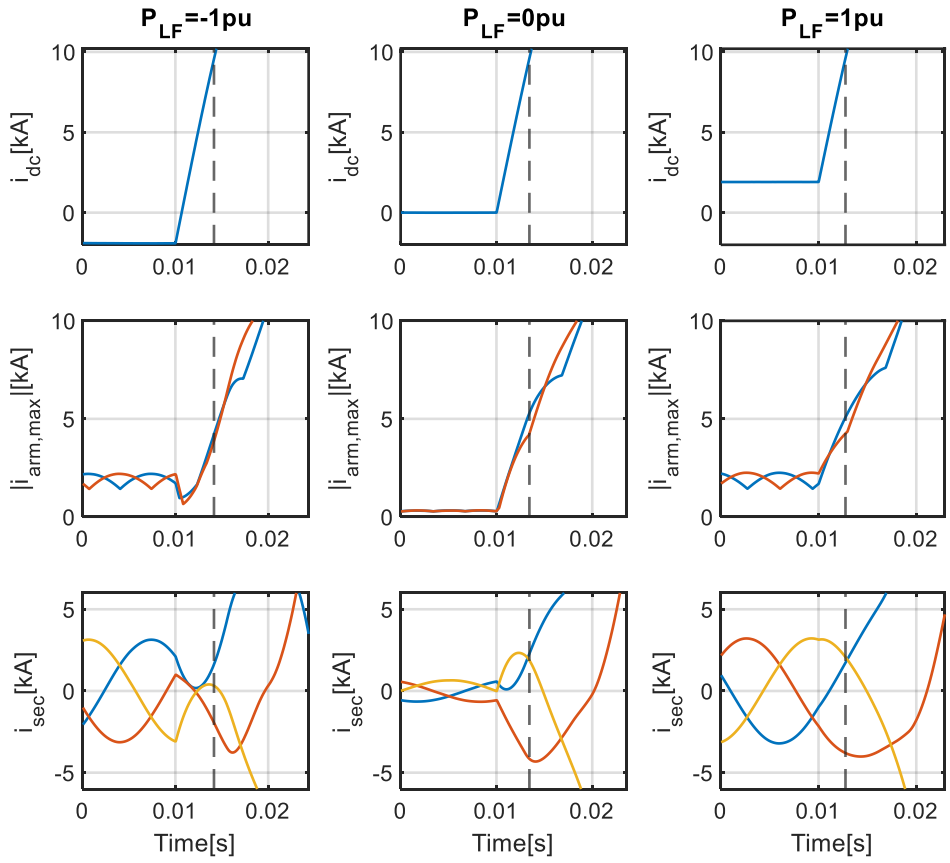


Figure 101 Evolution of DC currents, maximum of lower (red) and upper (blue) arm currents and secondary AC currents for different pre-fault load flows; L_{dc}=150mH, SCR=24GVA, $i_{dc,blk}$=5pu, T_r=100ms

Figure 102 shows a sensitivity analysis of maximum arm currents for different DC current blocking constraints depending on different pre-fault load flows and different DC reactor values.

→ $I_{dc,blk}$=2pu: The dimensioning scenario[11] for all DC reactor values is a positive load flow. As the DC current limit is very low, the dependence on AC currents is limited.

→ $I_{dc,blk}$=3pu: The positive load flow is not the dimensioning scenario for a DC reactor value higher than 500mH.

→ $I_{dc,blk}$=[4pu 5pu]: The negative load flow becomes dimensioning scenario for L_{dc}>500mH (4pu) and L_{dc}>350mH (5pu).

As a conclusion, different load flow scenarios need to be investigated to identify the highest arm current for a given DC current blocking constraint.

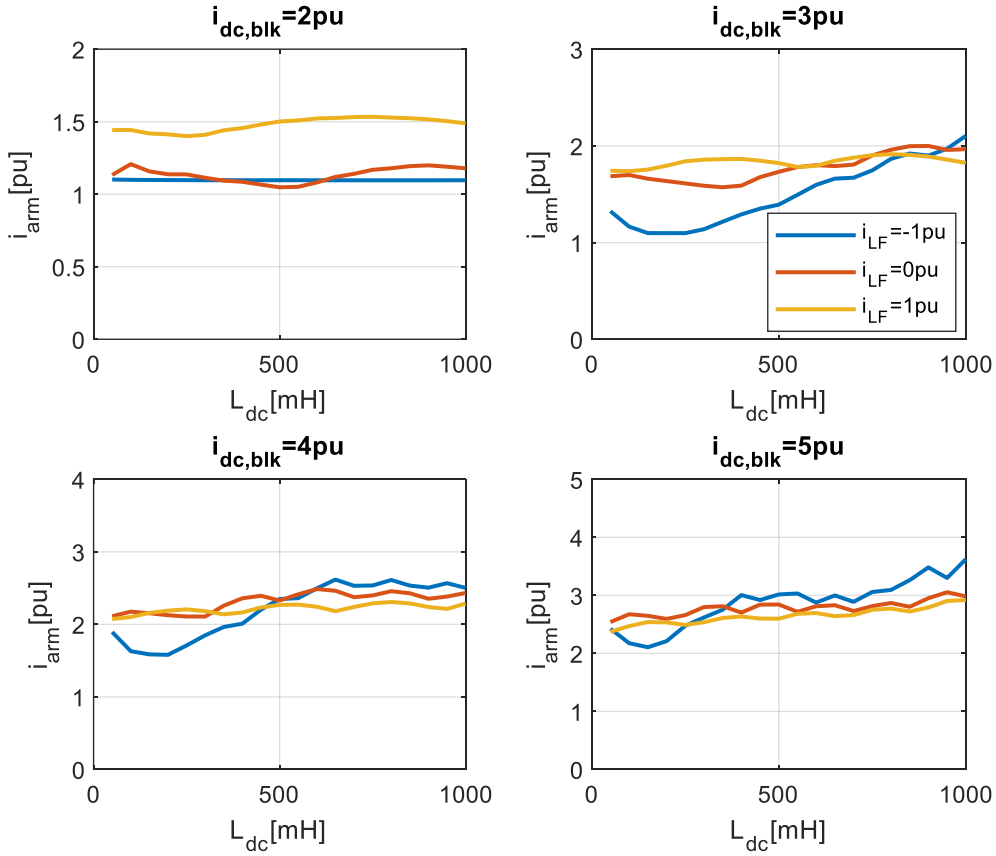


Figure 102 Sensitivity analysis of maximum arm currents for different DC current blocking constraints and different load flows; converter response time T_r=100ms

[11] Scenario that provokes the highest arm current for a given DC current blocking criteria.

7.2.1.4. Conclusions

The sensitivity analysis from previous sections underlined that the increase of arm currents during DC faults depends on several key parameters such as pre-fault load flow, control parameters and DC reactor size. The link between arm currents and DC currents is not straightforward and requires an in-depth investigation including the aforementioned aspects. It should be noted that control mode and control parameters of the converter have an impact on the maximum arm currents as well.

Figure 103 resumes the results of all sensitivity analyses of the previous sub-sections and indicates the maximum arm current for a given DC current blocking criterion and for a given DC reactor value.

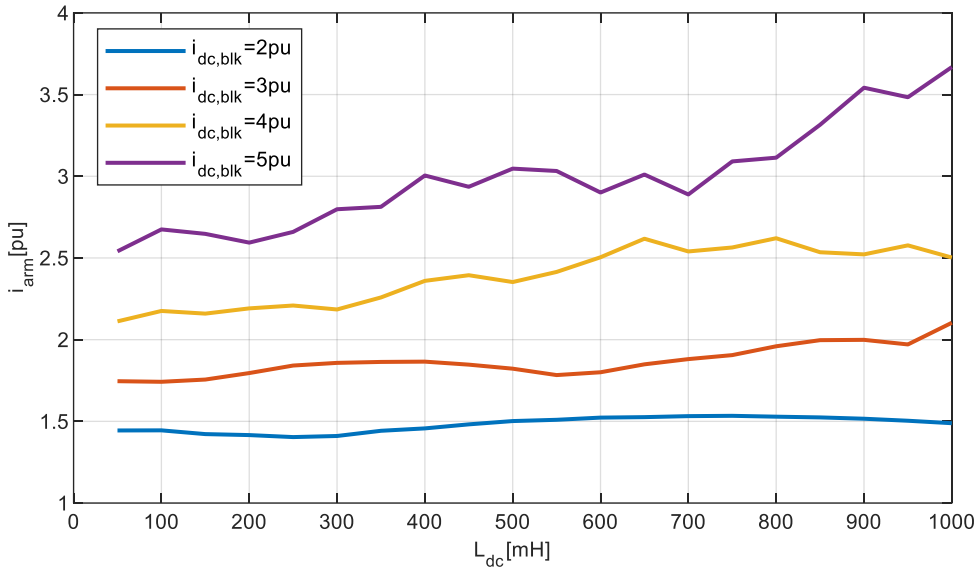


Figure 103 Maximum arm currents for different DC current blocking constraints and different load flows; converter response time T_r=100ms

Table 39 shows the relation between maximum arm current and DC blocking current criteria i_{dcblk}=[2 3 4 5] pu. In this study, it is assumed that some IGBT modules could sustain higher currents than 2pu. Therefore DC blocking currents of up to 5pu are investigated in this study.

Table 39 Maximum arm current for different DC current blocking criteria

DC blocking current criteria	Maximum arm current
2pu	1.5pu
3pu	2.1pu
4pu	2.6pu
5pu	3.7pu

A reliable and progressive rollout of the DC protection system requires to respect the blocking constraints of the converters in order to limit the loss of infeed during faults. The analysis has clearly shown that the arm

currents may vary significantly for the same DC fault as they are also dependent on AC side quantities. A DC current blocking criterion allows to dimension the protection system based on DC quantities that need to be withstood by all converters connected to the DC grid.

The analysis of DC current blocking criteria can feed into functional requirements for the MMC as indicatively shown in Figure 104, where the first current threshold is equal to the DC current blocking criteria ($i_{mmc1}=i_{dc,blk}$). The MMC must support the overcurrent i_{mmc1} during a time frame of the fault neutralization time $t_{mmc1}=t_N$. The second time constraint t_{mmc2} is determined by the fault interruption time which is further specified in section 7.6. The second overcurrent threshold i_{mmc2} is related to dynamics and control interactions after fault interruption and DC contingencies. The time t_{mmc3} refers to the settling time of the converters in the MTDC grid.

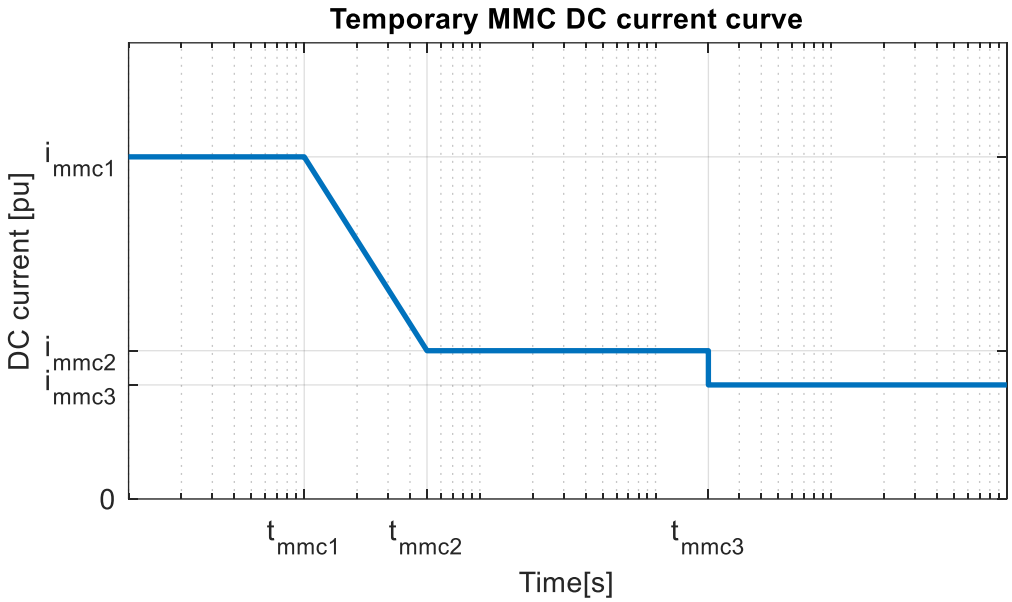


Figure 104 Temporary DC current curve for MMC at DC-PoC (indicative)

Table 40 Parameter ranges for MMC overcurrent ride through

ID	Symbol	Characteristic/Events	Range
110	i_dcblk	MMC need to remain connected until reaching DC current blocking criterion	[2-5] pu
119	i_mmc1	Identical to i_dcblk	[2-5] pu
120	i_mmc2	Dynamics and control interactions after fault interruption	[1.1-1.3] pu
121	i_mmc3	Steady-state operation	[1-1.1] pu
122	t_mmc1	Maximum rise time of fault current (related to fault neutralization time)	<0,01 s
123	t_mmc2	Related to fault current suppression time	<0,05 s
124	t_mmc3	Settling time after step changes	N/A

7.2.2. Undervoltage protection

A significant DC voltage drop implies that there is a problem in the system. Hence, in a PtP link the undervoltage indicator can be used to identify problems and, if they persist, to shut down the converter. However, in MTDC grids the DC voltage support by converters is more than necessary to restore from undervoltage after faults or other issues. On the other hand, technical limits of converters in terms of submodule discharge must be considered to avoid any damage and instability. However, a clear technical limit of the components as in the case of IGBT overcurrent protection does not exist for the undervoltage of submodules which leaves open the question of stability limits for both level of undervoltage and duration.

Figure 105 shows a simplified circuit of an MMC feeding a spoke fault. The DC reactors L_{dc} should be conceived so that blocking is avoided until fault neutralization by the DCCB. To simplify, it is assumed that the converter is the only contributor to the fault current (no interconnectors). In pre-fault state T_0, the MMC submodule capacitors are at rated energy level. At T_1, which is equal to the fault neutralization time, a certain amount of electrostatic energy of the capacitor has been transformed to magnetic energy stored in the DC reactor. The magnetic energy depends on maximum current at T_1 and on the DC reactor size. This leads finally to a certain undervoltage that will be further described.

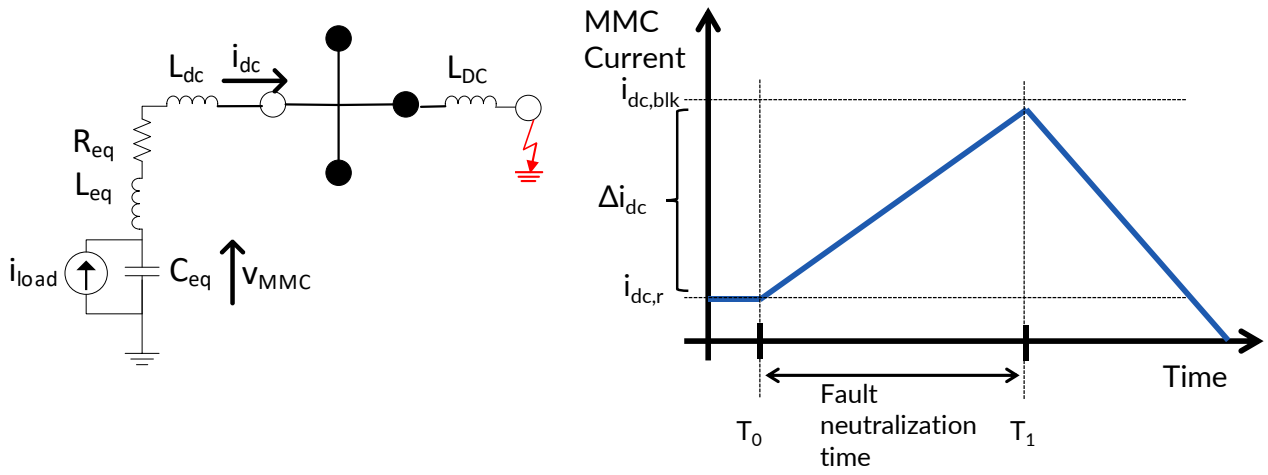


Figure 105 Simplified circuit for spoke fault representation (left) and schematic current behavior from fault inception to fault clearing

An analytical formula of energy balance between converter capacitance and magnetic energy stored in the inductors can be used to determine the undervoltage level from fault inception to fault neutralization assuming no resistive losses (R_{eq}=0).

$$E_{MMC,1} = E_{MMC,0} - E_{L,1}$$

$$E_{MMC,0} = \frac{1}{2} C_{eq} v_{dc,0}^2 \qquad E_{MMC,1} = \frac{1}{2} C_{eq} v_{dc,1}^2$$

$$E_{L,1} = \frac{1}{2}(2L_{dc} + L_{eq})\, i_{dc,blk}^2$$

$$v_{MMC,1} = \sqrt{2\, E_{MMC,1}/C_{eq}}$$

Figure 106 shows the results for the theoretical undervoltage of the MMC converter with use case parameters ($E_{MMC,0}$=40MJ) depending on the DC reactor and the authorized DC current blocking criteria. The analytical

results (solid lines) are compared with PSCAD simulation results (AVM-DC model). The analytical calculation shows a good approximation with small differences due to neglection of resistive parts. The choice of DC current blocking criteria has an important impact on the maximum undervoltage as it increases the maximum current in the DC reactor and as a result the magnetic energy stored in the DC reactor. Secondly, high DC reactors lead to an important undervoltage.

As a conclusion, both parameters should be chosen such that the temporary undervoltage of the converter during faults is limited to an acceptable value keeping the converter operational.

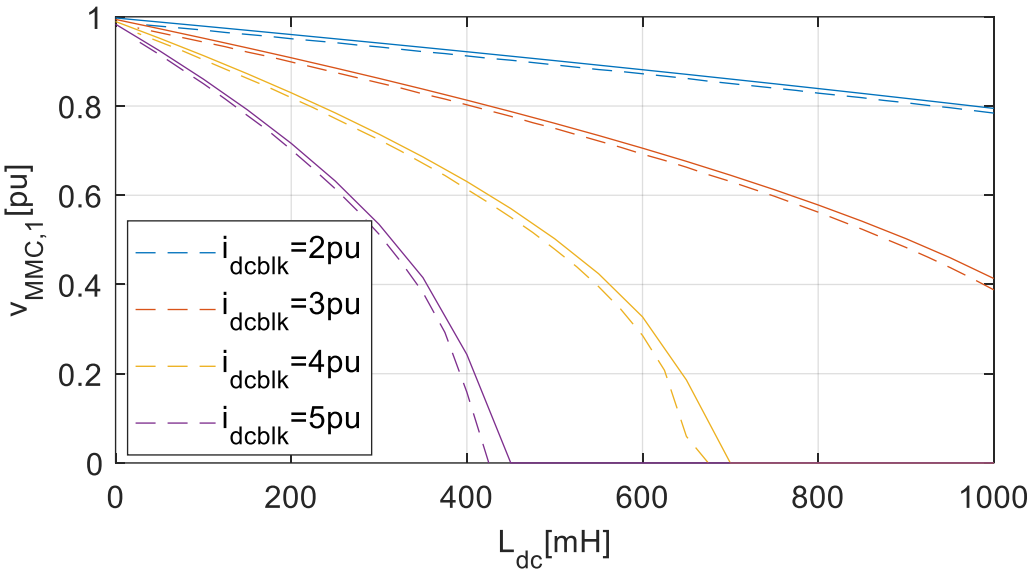


Figure 106 MMC undervoltage due to discharge in case of spoke fault depending on DC reactor size and DC current blocking criteria; Solid lines: analytic calculation, dashed lines: Results from PSCAD simulation with AVM-DC

7.2.2.1. Converter energy level

Another influencing factor is the energy rating of the converter. In fact, a high energy rating limits the voltage drop for a given DC current blocking criteria and DC reactor.

A sensitivity analysis on DC undervoltage limits and the link with converter energy level requirements will be carried out in the following considering three different converter energy levels: E_{mmc} = [20 40 100] MJ, where 40MJ is the base. Figure 107 shows the minimum voltage level for the different converter energy levels considering a DC current blocking criteria of 3pu. It is clearly visible that an increase of available converter energy can limit the submodule discharge importantly.

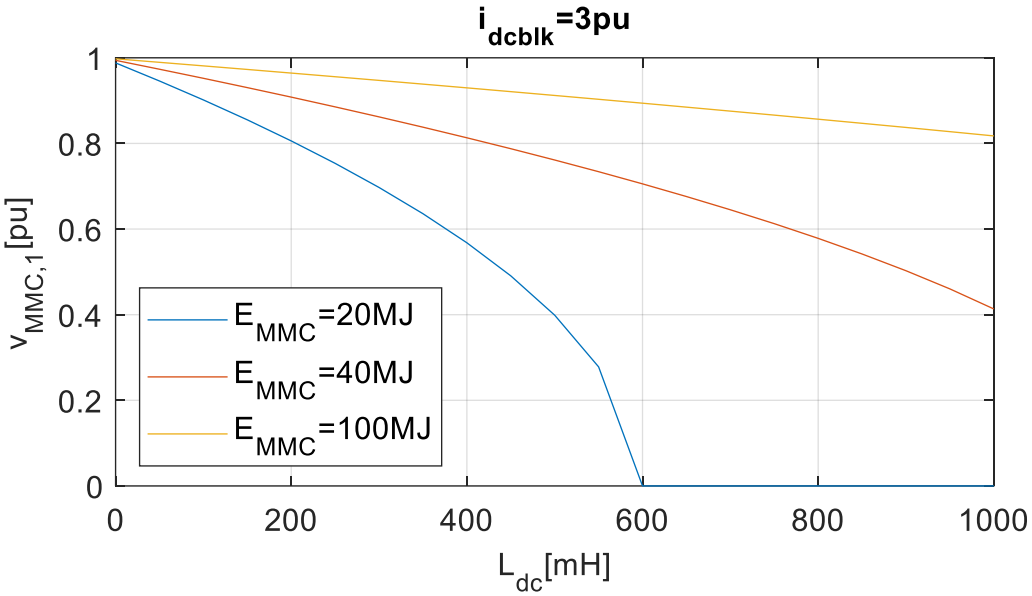


Figure 107 Maximum converter discharge considering different converter energy levels for a given $i_{dc,blk}$=3pu

The minimum converter energy level requirements for an exemplary submodule undervoltage limit of 0.5pu can be deduced from Figure 108. The converter energy level should be chosen in coordination with the DC reactor values at the node and the DC current blocking criteria.

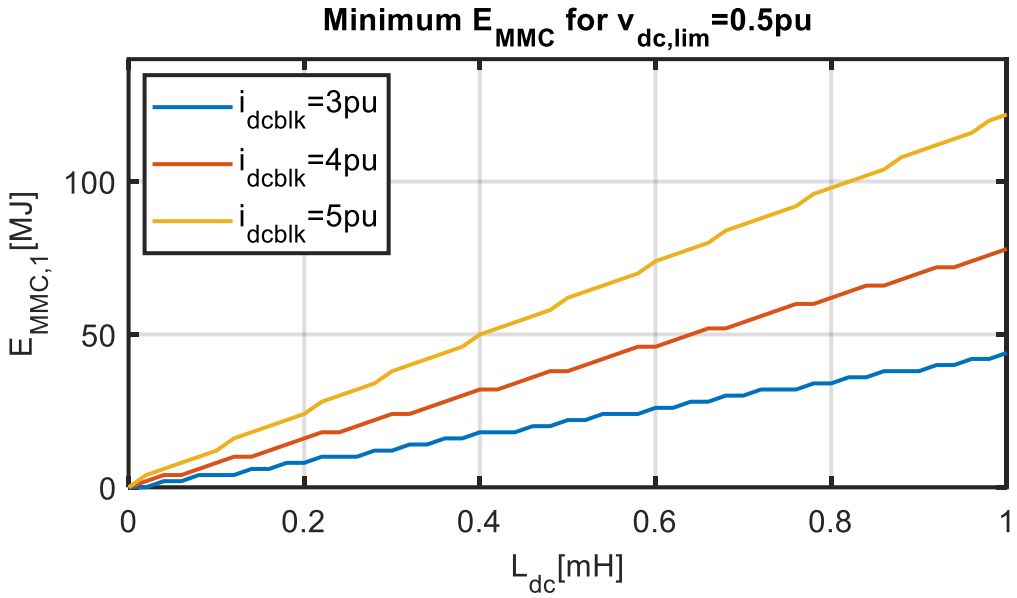


Figure 108 Minimum MMC energy level requirements for a submodule undervoltage limit of 0.5pu

7.2.2.2. Conclusions

The analysis showed that the following parameters have an important impact on the maximum discharge of the converter during DC faults:

- → DC reactor size
- → Converter energy level
- → Choice of DC current blocking criterion

For some combinations an important submodule voltage drop has been identified. This opens the question of technical limits for converter submodule discharge. The following two points should be considered:

- → Overmodulation: To what extent can overmodulation be accepted from the time of fault inception to fault clearing?
  - > Transient overmodulation during DC faults is difficult to avoid and is therefore acceptable if not enduring. The converter should be able to ride through the DC fault while keeping controllability without blocking.
- → Submodule power supply limits: A submodule will block if the voltage drops below a certain value. The reason is that all electronics within the submodule (gate drivers, protection logics etc.) rely on a power supply to run and this power is derived from the submodule itself.
  - > Submodule power supply limits should be respected during DC faults in order to keep the converter operational. However, the hard limit of undervoltage may depend on the specific converter and submodule design. A first conclusion is that a complete discharge (0% of rated voltage) is not acceptable. The reasonable limit should be chosen according to the submodule power supply limits (i.e. a minimum submodule voltage level of 1000V in order to ensure the gate drives).

Table 41 Functional requirements related to MMC undervoltage ride through during DC faults

ID	Functional requirement
General72	The converter should not block due to submodule undervoltage protection during DC fault clearing sequences if voltage remains within over- and undervoltage ride through profiles

Table 42 Parameters for MMC undervoltage ride through

ID	Symbol	Characteristic/Events	Range
125	u_dcblk	The MMC should remain connected until undervoltage limit is reached	

7.3. DC Fault Ride Through profiles

The aim of this section is to specify DC over- and undervoltage Fault Ride Through (FRT) profiles in amplitude and duration for the AC/DC converter at the DC-PoC.

The CENELEC guideline is considered as state of the art. In it, the AC FRT for an AC/DC converter station is defined as its capability of staying connected to the AC system and remaining in stable operation for a certain over- and undervoltage profile (OVRT and UVRT) [26] . Examples of generic OVRT and UVRT profiles of an AC/DC converter station are shown in Figure 109. Note that depending on pre-fault conditions or type of faults (e.g., symmetric vs unsymmetric AC faults), multiple fault ride through characteristics can be given.

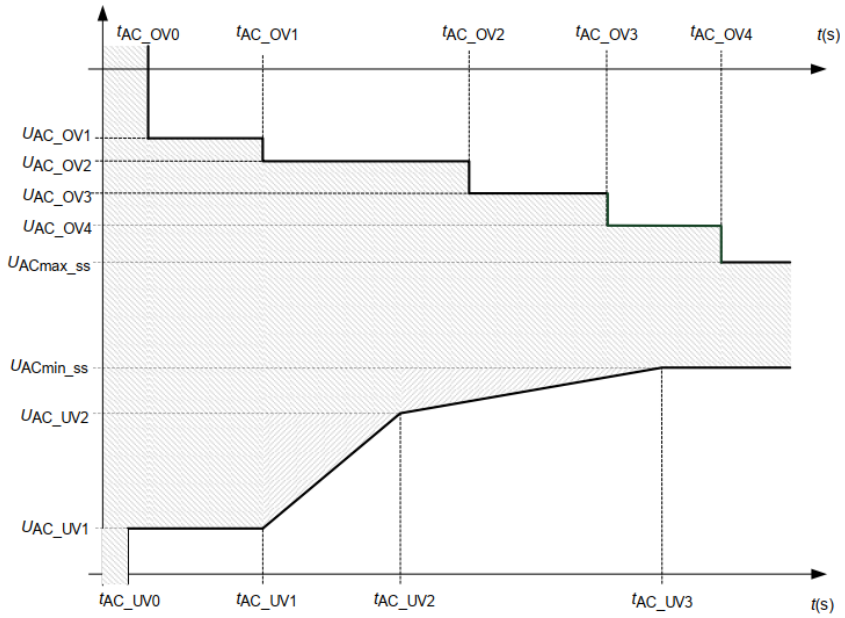


Figure 109 Exemplary generic AC Over- and Under Voltage Ride Through profile of an AC/DC converter station [26]

The DC FRT is considered as the capability of the AC/DC converter to stay connected at the PoC-DC and remain in stable operation during an insulation fault appearing at another PoC-DC for a certain over- and undervoltage profile. In other words, the MMC should be unblocked and controllable if the voltages at the PoC-DC remain within the DC FRT profile.

To define parameter ranges for the DC FRT, dimensioning scenarios and technical limits of DC grid components have been evaluated. Temporary over- and undervoltages in DC grids may occur due to various reasons. The time frame may vary from a few milliseconds (transient stress) to several hundreds of milliseconds (protection coordination and control dynamics) and even to several seconds (load flow considerations). The following events need to be considered for over- and undervoltage specifications:

→ DC faults

> Traveling wave reflections at inductive terminations may lead to transient voltage reversals at the cable end. The voltage may decrease locally to -1pu.

> From fault inception to fault neutralization, partial discharge of the DC grid occurs (i.e., converter submodules and cable stray capacitance). The converter submodule capacitance discharge is further

investigated in section 7.2.2.

→ DC circuit breaker operation: during fault current suppression (from fault neutralization to current zero), the DC circuit breaker imposes a TIV that needs to be withstood by other components in the grid. The fault current suppression time is further investigated in section 7.5.

→ DBS operation in case of inverter blocking or spoke fault: DC grid components are exposed to an overvoltage of at least the DBS overvoltage activation threshold during the time that is required to ramp down the wind farms. Both DBS activation time and amplitude are further investigated in section 7.7.

→ Uncoordinated power step changes lead to dynamic over- and undervoltage as well as steady-state DC voltage deviation. The methodology of the primary DC voltage control (droop control) to contain the steady-state DC voltage will be investigated in 6.3.2. Dynamic DC voltage deviations under the primary DC voltage control is further specified in section 6.3.5.

→ Steady-state voltage ranges are specified in 6.1.

→ Energization processes of parts of the DC grid and dedicated temporary over- and undervoltage are specified in section 8.2 and 0.

Figure 110 shows a proposal for DC-FRT profile (DC pole-to-ground voltage) considering over- and undervoltage with characteristic times and per unit voltage. Table 43 and Table 44 give indicative ranges and dimensioning events for DC-FRT profile.

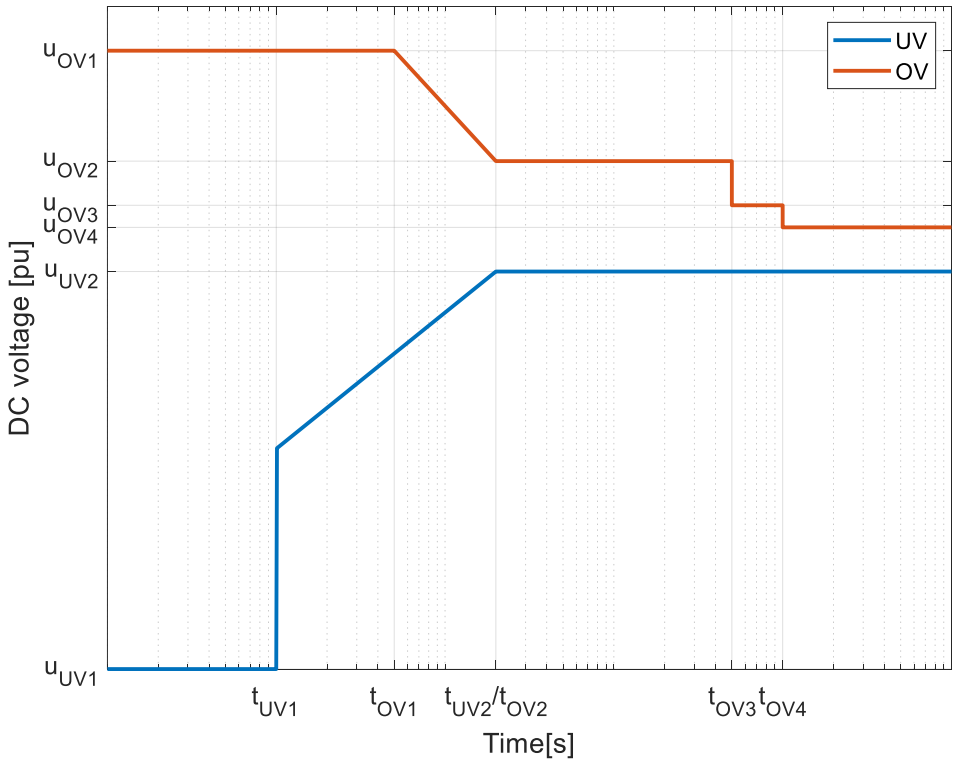


Figure 110 Proposal of DC-FRT profile for HVDC grid systems

Table 43 DC-FRT parameters

ID	Symbol	Characteristic/Events	Range
80	U_{OV1}	DCCB operation, switching transients, trip of converter	1.5-1.8pu
81	U_{OV2}	Settling time after fault clearing Energization transients	1.05-1.4pu
82	U_{OV3}	Trip of converter, DBS activation time, Droop full activation time (Primary DC voltage control)	1-1.1pu
83	U_{OV4}	Steady-state DC voltage (upper limit), secondary DC voltage control	1pu
86	t_{OV1}	DCCB operation, switching transients, trip of converter	1-50ms
87	t_{OV2}	Settling time after fault clearing	<1s
88	t_{OV3}	Trip of converter, DBS activation time, Droop full activation time (Primary DC voltage control)	<5s
89	t_{OV4}	Steady-state DC voltage (upper limit), secondary DC voltage control	<10s

Table 44 DC voltage range parameters - temporary undervoltages

ID	Symbol	Characteristic/Events	Range
84	U_{UV1}	Voltage levels from fault inception to fault neutralization	[-1 0,5] pu[12]
76	U_{UV3}	Steady state operation Energization transients	[0.8-1] pu
77	t_{UV1}	Voltage levels from fault inception to fault neutralization	[1-10] ms
78	t_{UV2}	DC fault voltage recovery	Several hundreds of ms

Within this report, a sensitivity analysis is carried out to assess the impact of the UVRT profile parameter on the design of the protection devices. In particular, the analysis is focused on the parameters U_{UV1} and t_{UV1} (see Figure 110) from fault inception to fault neutralization, which are linked to MMC undervoltage protection examined in section 7.2.2. It is worth noting that the definition of the DC-FRT profile parameters relies on

[12] Value of -1 pu is related to traveling wave reflections at inductive terminations as already explained above. Value of 0.5 pu is related to a possible SM undervoltage limit that could increase the minimum acceptable voltage level at MMC output. Indeed, all electronics within the submodule (gate drivers, protection logics etc.) rely on a power supply to run and this power is derived from the submodule itself. If submodule voltage drops below submodule electronic active threshold of about 1000V, no action can be done on submodule anymore (information from client).

several factors which can be system dependent or converter technology dependent. Further in-depth investigations are needed for the definition of such parameters as proposed in the next steps section.

The DMR is connected to the grounding point of the converter and should be dimensioned to withstand temporarily the maximum voltage at the grounding point that occurs during DC faults due to the ground return current. This voltage level should be designed such that transient voltage levels from the highest grounding impedance can be withstood. In case of grounding via surge arresters, the clamping voltage should be withstood. The DMR should further sustain permanently the voltage drop when operating in asymmetrical monopolar operation. The voltage drop depends mainly on the cable characteristics and the length. The voltage level in steady-state operation is further investigated in section 6.1.

The temporary DC voltage curve for the DMR is depicted in Figure 111. Different from the pole voltage, the DMR voltage is not indicated in per unit but in SI. This is due to the fact that the DMR is not directly related to the pole voltage rating. It is further expressed in absolute values since the temporary DC voltage curve for the DMR is symmetric and applies for positive and negative voltages.

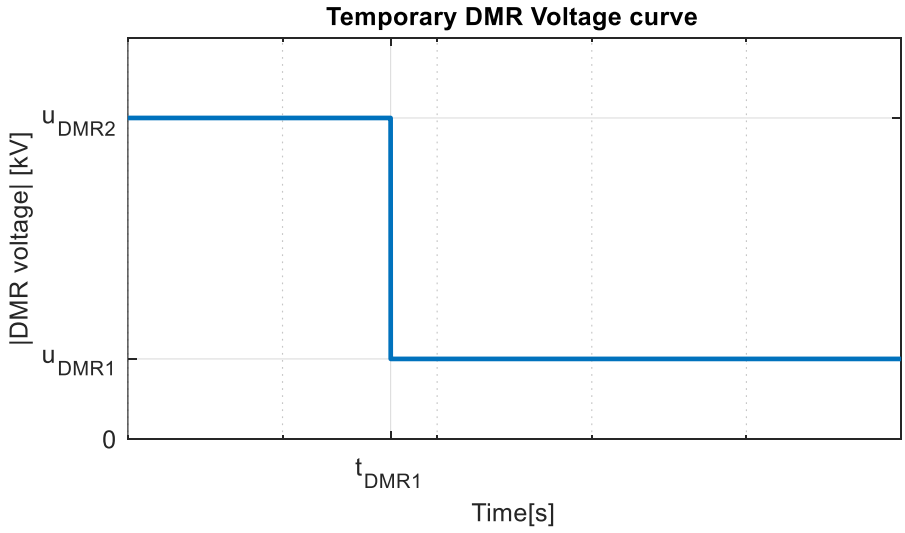


Figure 111 Temporary DC voltage curve (absolute values) for dedicated metallic return (indicative)

Table 45 Temporary DC voltage range parameters for the dedicated metallic return

ID	Symbol	Characteristic/Events	Range
115	U_{DMR1}	Steady-state voltage in asymmetrical monopolar configuration	Few tens of kV, depending on cable characteristics and conductor length, see section 6.1
116	U_{DMR2}	Transients due to DC faults and fault return currents through grounding scheme Transients due to switchgear operation after DMR fault and/or neutral/earth reconfiguration.	Depending on grounding scheme & clamping voltage. See section 9.1.7 for DMR fault.
117	t_{DMR1}	Time from fault inception to fault current suppression at high voltage pole	Several tens of ms, see section 7.5

The following hypotheses apply:

- → The considered DC grid in this study is fully cable based. Thus, overhead lines are not part of this study and specifications for de-ionization times and dedicated voltage levels are not further specified.

- → Detailed insulation coordination study as well as arrester design is not in the scope of this study. It is assumed that overvoltages higher than the DC circuit breaker TIV will be limited by the arrester clamping voltage.

7.4. DC Circuit Breaker operating time and DC reactor specifications

The DC Circuit Breaker and DC reactor specification is based on a systematic approach considering primary and backup sequences for the given hub topology as shown in Figure 112. The hub consists of at least one offshore converter, and one spoke and two internal interconnectors. The interconnectors may be realized in a later stage of the project such that the exact device and topology is not known. The following options must be considered:

- → Short interconnector distance (0-50km)
- → Long interconnector distance (50-400km)
- → Offshore converter connection

The cable distance has an impact on the equivalent capacitance and hence on the fault current contribution. If an additional converter is connected the additional fault current contribution must be considered in the design of DCCB and DC reactor. It is further important to consider the blocking constraints imposed by the protection strategy as listed in Table 46.

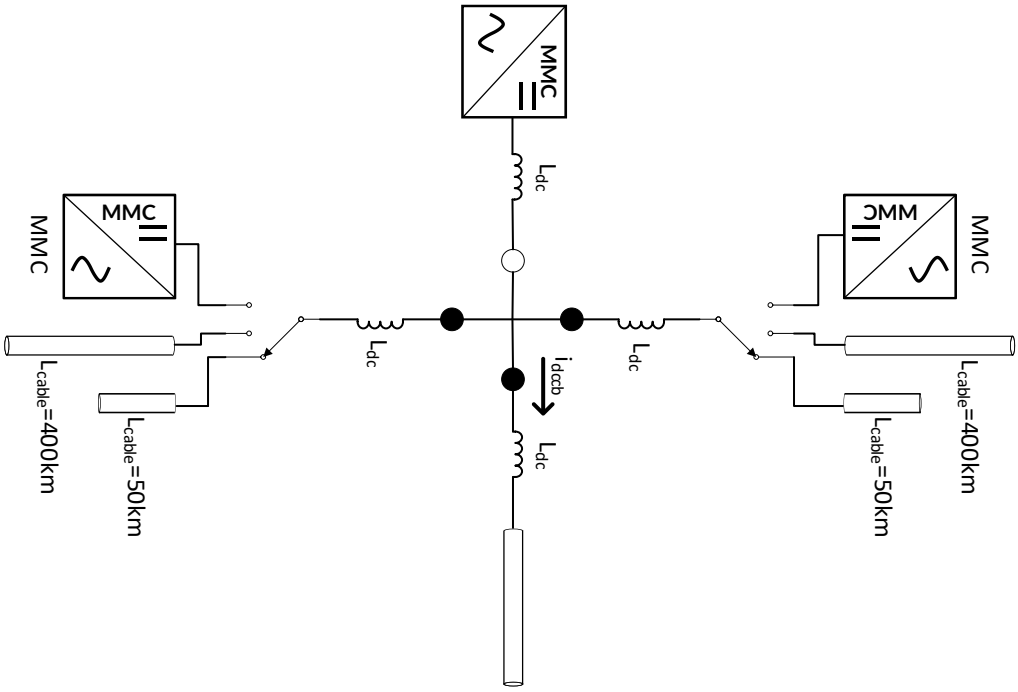


Figure 112 Hub topology with possible interconnections: long cable, short cable, converter

Table 46 Blocking criteria for primary and backup protection scenarios

Blocking criteria	Busbar fault	Line fault II	Line fault spoke (connection to shore)	Line fault II + breaker failure	Line fault spoke (connection to shore) + breaker failure	Line fault spoke (connection to shore) + breaker failure onshore
Connected MMC WF	Allowed	Not allowed	Not allowed	Allowed	Allowed	Not allowed
Adjacent MMC WF	Not allowed	Not allowed	Not allowed	Not allowed	Not allowed	Not allowed
MMC spoke (onshore converter)	Allowed	Not allowed	Allowed	Allowed	Allowed	-
MMC spoke (onshore converter) With DC breaker	Not allowed	Not allowed	Not allowed	Not allowed	Not allowed	Allowed

7.4.1. Methodology

The above defined blocking constraints needs to be respected for all possible future grid extensions and grid configurations (i.e., disconnection of interconnectors) considering primary and backup sequences. This implies that the fault needs to be neutralized before the DC current blocking criteria $i_{dc,blk}$ is reached. The different time periods to be considered from fault inception to converter blocking are illustrated in Figure 113 for primary sequence (left) and backup sequence (right). The definitions of the time periods are given by Table 47. It should be noted that the time from fault inception to MMC blocking mainly depends on the di/dt, thus on the DC reactor value.

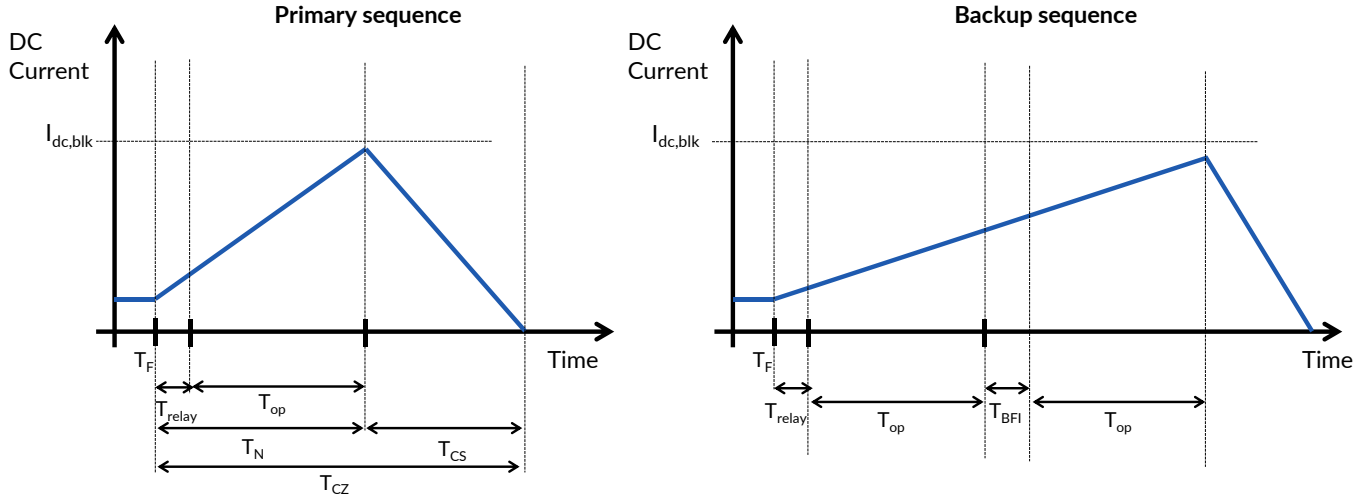


Figure 113 Blocking time constraint for primary sequence (left) and backup sequence (right)

Table 47 Definition of time periods during fault neutralization

Parameter	Description
T_F	Fault inception[13]
T_{relay}	Fault inception to trip order
T_{op}	Trip order to fault neutralization
T_{BFI}	Breaker failure Identification time
T_N	Fault neutralization time
T_{CS}	Fault current suppression time
T_{CZ}	Fault current zero time

The conditions to avoid MMC blocking for primary and backup sequences are respectively defined as $T_{\mathrm{blk,prim}}(L_{dc}) > T_{\mathrm{N}}$ and $T_{\mathrm{blk,backup}}(L_{dc}) > T_{\mathrm{relay}} + 2T_{\mathrm{op}} + T_{\mathrm{BFI}}$ where $T_{\mathrm{blk,prim}}$ is the time during which the MMC connected to the node is not allowed to block during primary sequence and $T_{\mathrm{blk,backup}}$ is the time during which an adjacent MMC is not allowed to block during a backup sequence as defined in Table 46. Based on this, the conditions for the DCCB operating time can be defined as follows:

$$T_{op,prim} < T_{blk,prim}(L_{dc}) - T_{relay}$$

$$T_{op,backup} < \frac{T_{blk,backup}(L_{dc}) - T_{BFI} - T_{relay}}{2}$$

7.4.2. Simplistic Test Benchmark

For the primary protection sequences the offshore converter is allowed to block in case of busbar fault but is not allowed to block for spoke and interconnector faults. The dimensioning blocking constraint that applies for a primary sequence in a hub topology with two interconnectors as shown in Figure 112 is a case where one out of two interconnectors is disconnected. This can be due to multiple reasons such as future extensions or maintenance. The case of two interconnectors is also possible if the system returns to a point-to-point operation. In fact, this configuration leads to the fastest increase of the MMC current as other fault current contributions would limit the voltage drop at the busbar and hence limit the contribution of the MMC. However, the blocking constraints should apply only if the converter can be kept in operation. In point-to-point operation in combination with a fault on the spoke the entire pole needs to be shut down such that blocking of the offshore converter is acceptable. It is important to consider that a fault at the beginning of the spoke does not lead to the steepest increase of fault current as a fault inside the spoke imposes a negative voltage at the cable end due to the reflection coefficient of the incident traveling wave at an inductive termination (see 0, traveling wave generator model).

[13] In this context fault inception is the time of fault arrival at the relay.

A sensitivity analysis has been carried out to investigate if the STB remains valid compared to the real case of one interconnector connected and variation of fault distance on the spoke (considering traveling wave propagation). Figure 114 shows the virtual mock-up for both topologies. For topology a) the spoke length is varied. The results are shown in Figure 115. The upper curves show the fault current evolution whereas the bottom curves show the error between STB and curves obtained from topology (a). The rise of fault current of the STB (blue curve) is very similar to the other curves obtained from topology (a). For the sensitivity analysis a range of DC reactor from 100mH-500mH and a spoke length from 50km to 500km has been considered. The maximum positive errors in a time frame of 10ms after fault inception are listed in Table 48. The maximum error is of 0,34kA.

Based on this analysis it can be concluded that the proposed STB, see Figure 114 (a) shows satisfying results. The maximum error will be compensated by a safety margin i_{margin}=0,5kA. Hence, the threshold for the MMC is reduced to $i_{mmc,th} = i_{dc,blk} - i_{margin}$.

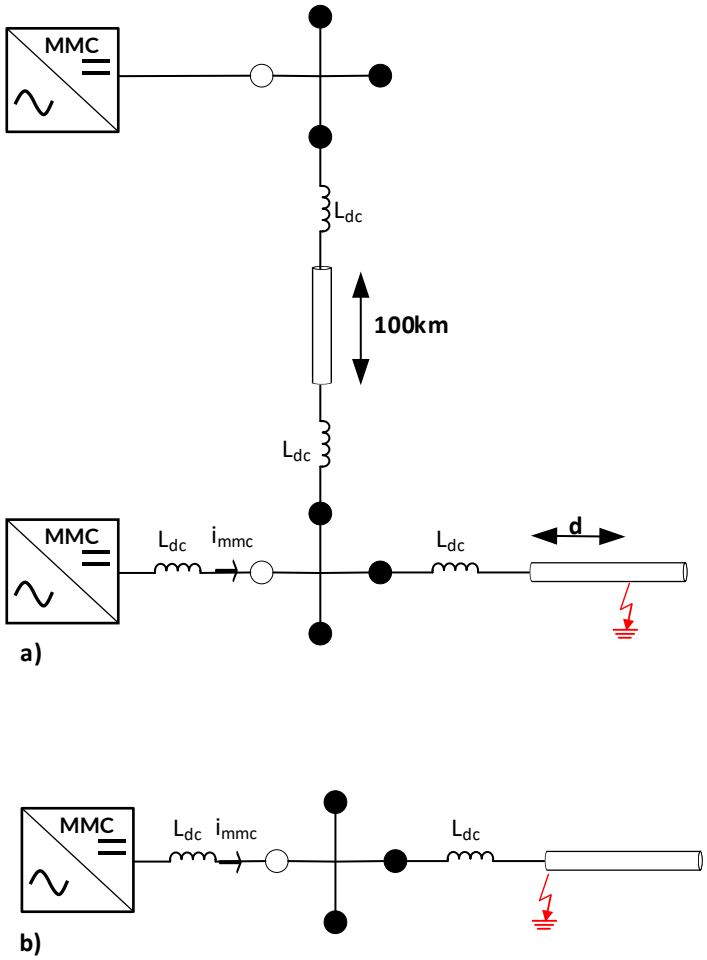


Figure 114 Mock-up for sensitivity analysis; a) Real case with one interconnector and variation of fault distance on spoke, b) Proposed STB without interconnector and with fault at beginning of cable

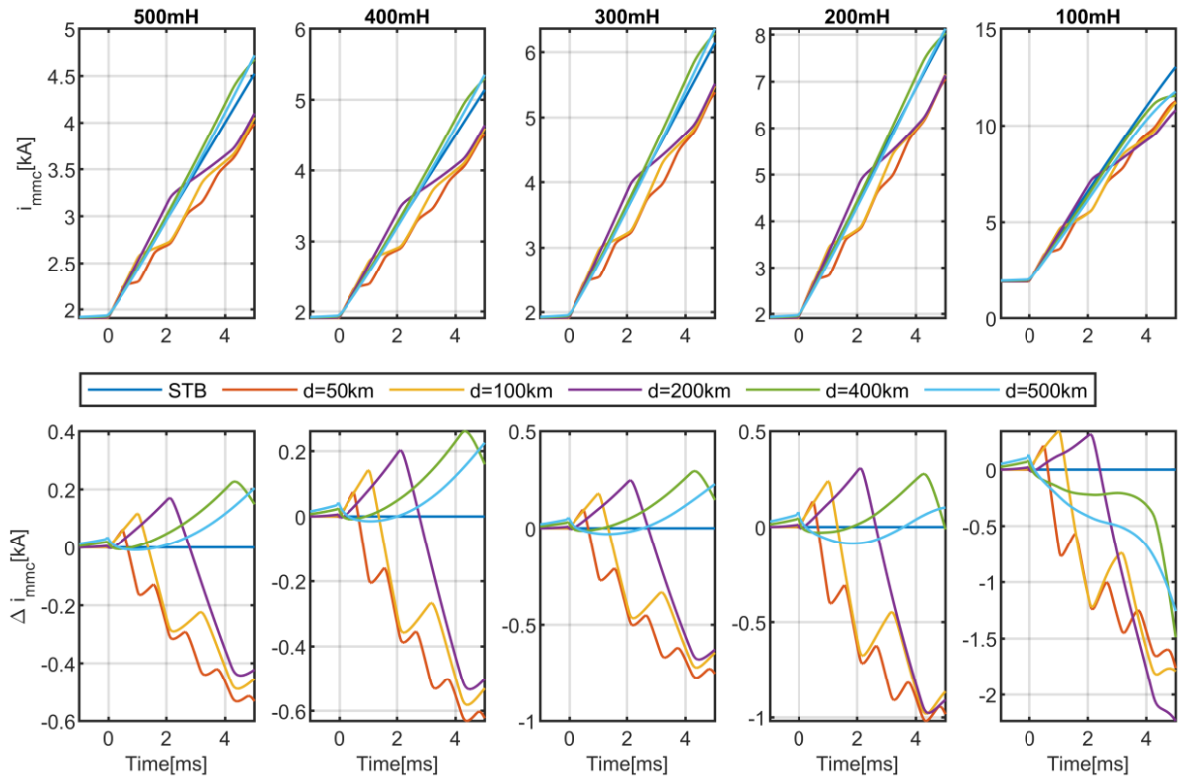


Figure 115 Comparison of STB (blue curve) and sensitivity analysis (fault distance d=[50 100 200 400 500] km

Table 48 Maximum error between STB and topology (b) for a time of 10ms after fault inception in kA

		L_dc [mH]				
		500	**400**	**300**	**200**	**100**
Fault distance [km]	**50**	0,06	0,07	0,10	0,13	0,21
	100	0,12	0,14	0,18	0,24	0,34
	200	0,17	0,20	0,25	0,31	0,31
	400	0,23	0,26	0,29	0,28	0,02
	500	0,24	0,26	0,26	0,10	0,07

The PSCAD implementation of the STB consists of the AVM DC model with a pre-fault load flow of 1pu. The model is connected in series with two DC reactors. A variation of the following parameters is carried out:

- DC reactor: L_{dc}
- DC current blocking criteria: $i_{dc,blk}$

At each iteration the blocking time $T_{blk,prim}$ (L_{dc}, $i_{dc,blk}$) is retained. Finally, the operating time $T_{op,prim}$ is calculated by subtracting the relay time.

Another STB is necessary to take into account the backup scenarios if dimensioning. The highest constraint is imposed by a spoke fault in combination with a DCCB opening failure. In that case, the closest MMC is allowed

to block but the adjacent MMC is not allowed. In order to provide a generic approach, the interconnector length is set to zero. In this way, the adjacent MMC is closest to the spoke fault and shows the highest possible increase of fault current. The spoke of the adjacent MMC and a potential second interconnector are not represented as they would limit the contribution of the MMC (similar to reasoning for primary sequence). The corresponding STB is shown in Figure 116.

The PSCAD implementation consists of the closest MMC, the adjacent MMC and the following DC reactors:

- 1 DCR at spoke
- 3 DCR between adjacent MMC and busbar (1 DCR at MMC output and two at interconnector)
- 1 DCR between closest MMC and busbar

A simplified blocking scheme is used for the closest MMC as it will reach blocked state before the adjacent one. The simplified blocking scheme consists of bypassing the equivalent capacitor when the DC current blocking criteria is reached.

Similar to the STB for primary protection, a variation of DC reactors and DC current blocking criteria is carried out. Finally, the required operating time $T_{op,backup}$ is calculated based on the equation provided in 7.4.1. It should be noted that the breaker failure identification time T_{BFI} is an additional time section to be considered for the backup protection.

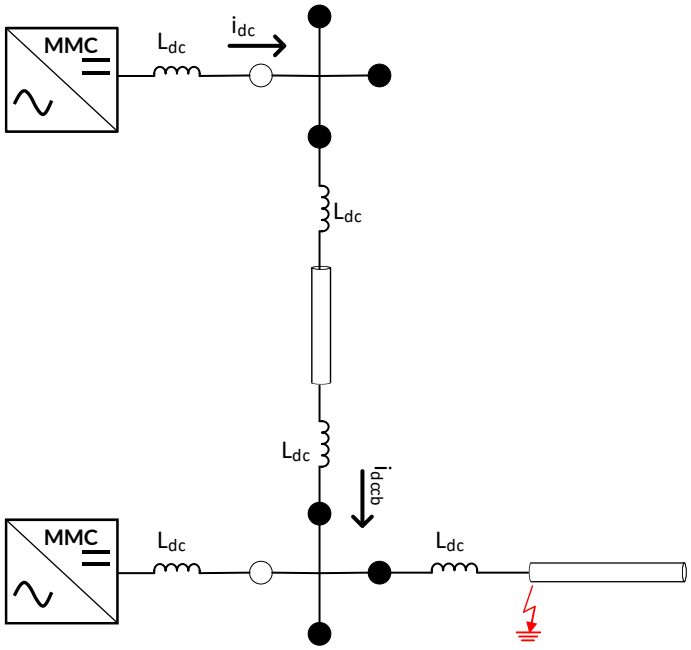


Figure 116 STB for determination of DCCB operating time in case of backup protection related to spoke fault

To obtain the dimensioning value $T_{op}(L_{dc}, i_{dc,blk})$, the smaller value out of primary and backup protection STB is retained.

In the case of a DCCB installation at the onshore side of the spoke the STB the dimensioning primary protection is a fault at the onshore side of the spoke. In this case the MMC is not allowed to block. The STB for the specification of DCCB operating time is similar to the one for offshore converters except that only one DC reactor is situated between the converter and the fault as shown in Figure 117. The traveling wave generator is connected to the model to investigate the dimensioning fault distance.

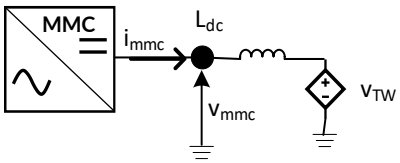


Figure 117 STB for DCCB operating time definition at onshore converter

7.4.3. Results

The DCCB operating time requirements for different DC reactor values and different DC current blocking criteria for DCCBs located at the offshore side are shown in Figure 118. Obviously a lower i_{dcblk} imposes a faster DCCB operating time. In other words, the DCCB operating time can be significantly relaxed for an identical DC reactor value. Taking L_{dc}=300mH as an example, the DCCB operating time is of 1.64ms for i_{dcblk}=2pu and of 9.18ms for i_{dcblk}=5pu. In this case the relay time and the breaker failure identification (BFI) time are set to 0.5ms and 1ms respectively. It should be noted that with increasing BFI time the number of dimensioning backup scenarios increases especially for low inductance values, whereas for T_{BFI}=0ms the primary scenario is dimensioning for the whole range of DC reactors. If the backup scenario is dimensioning, it is possible that the blocking time is smaller than the sum of relay time and BFI time. In other words, the converter blocks before fault and breaker failure have been identified. This leads to a non-feasible DCCB operating time requirement. Therefore, DC reactor values of less than 120mH, 60mH, 40mH and 40mH for 2, 3, 4 and 5pu of i_{dcblk} are not possible. Further considering an operating time of 1.5ms as a minimum the minimum DC reactor requirement is of 80mH.

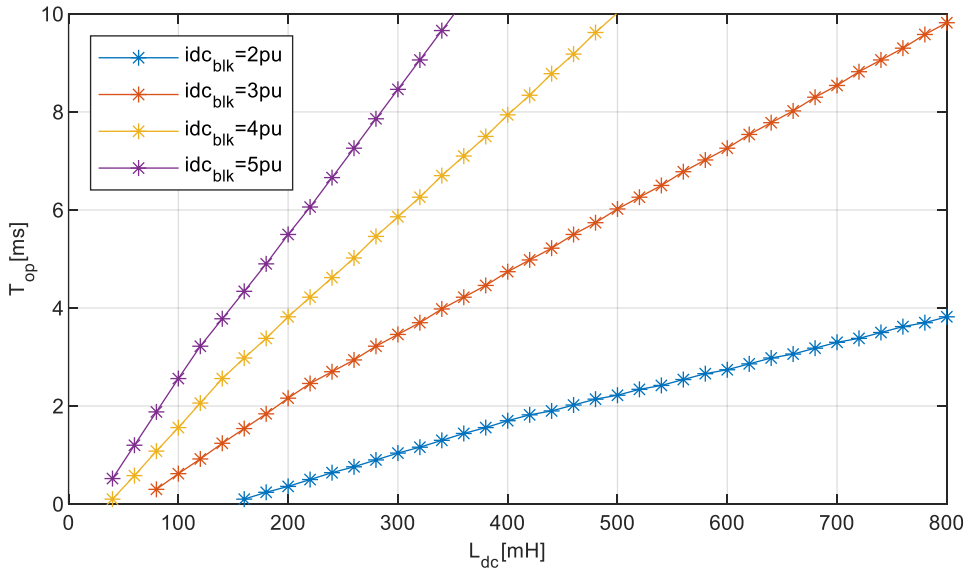


Figure 118 Required DCCB operating time offshore side to respect blocking constraints for a given L_{dc} and i_{dcblk}; T_{relay}=0.5ms, T_{BFI}=1ms

The DCCB operating time requirements at the onshore side are shown in Figure 119. The steepness of the curves is an indicator to what extent a higher DC reactor value provides a relaxed DCCB operating time. For $i_{dc,blk}$=2pu the curve is continuously flat. Even for a DC reactor value of 800mH a DCCB operating time of 1,3ms is required. Compared to the offshore requirements the DCCB operating requirements for a given DC reactor are shorter due to the following reasons:

→ Only one DC reactor is located between fault and converter instead of two DCR at the offshore side

→ The traveling waves of distant faults have an important impact on the increase of fault current

The second bullet point is underlined by the results shown in Figure 120. For all combinations of DC reactor and DC current blocking constraints the dimensioning case is not the closest fault at the direct output of the converter. It should be noted that for the calculation of the operating time the dedicated dimensioning scenario (worst case) has been considered. The bend in Figure 119 is due to the impact of the traveling waves which lead to steeper increase of fault current. If the blocking limit of the converter is reached due to the first traveling wave it has an important impact on the blocking time and hence on the DCCB operating time. For higher idcblk it is possible that the blocking current is reached only by the 2nd or 3rd traveling wave. In that case the steeper increase is compensated which leads to a more relaxed DCCB operating time (see Figure 33)

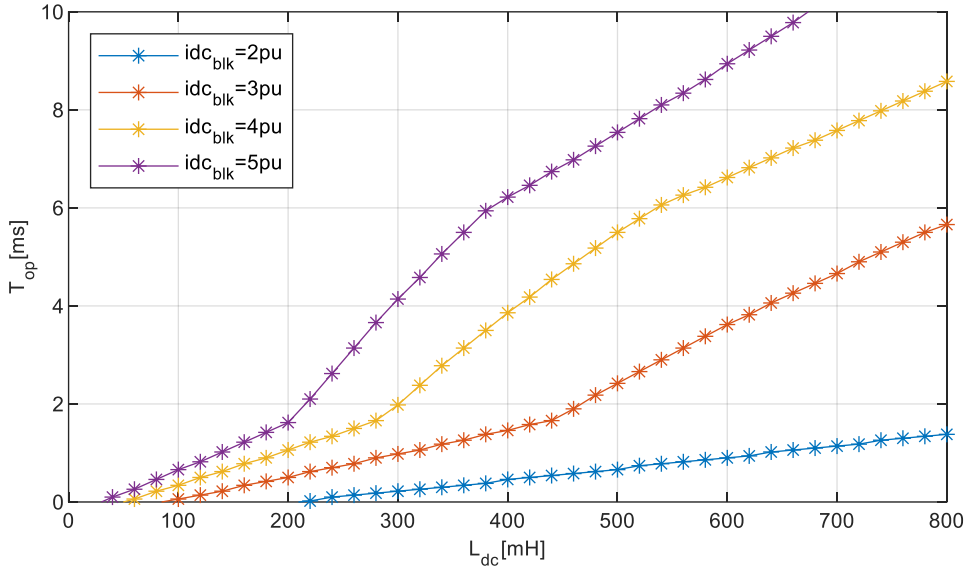


Figure 119 Required DCCB operating time onshore side to respect blocking constraints for a given L_{dc} and i_{dcblk}; T_{relay}=0.5ms

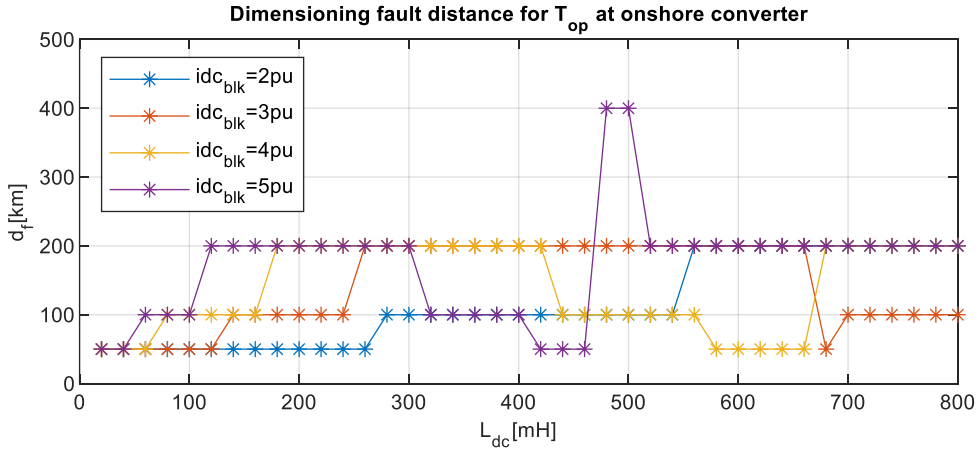


Figure 120 Dimensioning fault distance for DCCB operating time at onshore converter

7.4.4. Conclusion

Table 49 Functional requirements related to DCCB fault neutralization

ID	Functional requirement
General65	The building blocks should be equipped with sufficient fault current limiting devices in order to 1) avoid any damage on the components, 2) respect MMC blocking criteria during primary and backup protection sequences, 3) respect the DC system short circuit level while ensuring the transient stability of the DC grid.
General52	The overall DC fault neutralization time of fault separation devices should be specified. This includes DCCB operating time and relay time.

Table 50 Parameters related to DCCB fault neutralization

ID	Symbol	Characteristic/Events	Range
93	T_neu	Time from fault inception to fault neutralization (Peak TIV)	T_relay+T_op
94	T_relay	Time from fault inception to trip order	[0,5-3] ms
98	L_dc	DC reactor	[80-800] mH
107	T_op	DCCB operating time	[1,5-10] ms
109	T_BFI	Breaker failure identification time	[0,5-3] ms

7.5. DCCB current breaking capability specifications

7.5.1. Methodology

In this section the methodology to determine the DCCB current breaking capability (CBC) requirements is described. Considering the hub configuration shown in Figure 112 and the possible uncertainty of future grid extensions, the worst case of fault current contribution must be taken into account. This implies that not only elements of the existing grid but also fault current contributions from future devices must be considered. The reference fault scenario for this analysis is a spoke fault at the offshore side. In this way interconnectors and adjacent converters actively contribute to the fault current.

7.5.2. Simplistic test benchmark

The STB to determine the CBC for primary protection is shown in Figure 121. It consists of the offshore converter represented by an AVM DC model, two interconnectors with connections of ideal voltage sources of rated DC voltage and a spoke connection. A DC reactor of identical size is installed at each connection. The spoke is replaced by the traveling wave generator model (see section 5.4) in order to simulate different fault distances and to take into account the voltage surges imposed by traveling wave propagation. In fact, a distant fault might lead to a temporarily higher fault current. The current i_{spoke} is measured at the spoke as this is the fault current to be interrupted by the DCCB during primary protection. At each iteration $i_{CBC,prim}$ is defined in function of L_{dc}, i_{dcblk} and the required operating time to respect blocking constraints T_{op} (see section 7.4.2).

$$i_{CBC,prim}(L_{dc}, i_{dc,blk}, T_{op}) = \max\left(i_{spoke}(t)\right), t \in [T_F, T_N\ ]$$

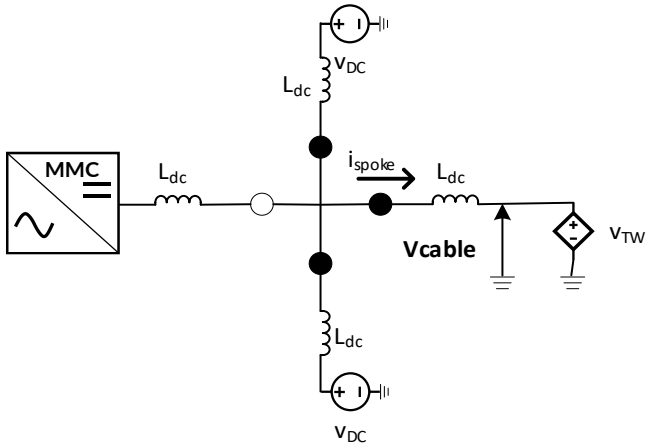


Figure 121 STB for CBC specification during primary protection: Spoke fault with ideal DC voltage sources for all interconnectors

A spoke fault with breaker failure is considered as the worst case for backup protection. The DCCB located at the interconnector needs to open after breaker failure identification T_{BFI} plus the considered operating time of the breaker that failed to open. The maximum current to be interrupted $i_{CBC,backup}$ is a function of DC reactor, DC current blocking criteria and DCCB operating time and is defined by the following equation.

$$i_{CBC,backup}(L_{dc}, i_{dc,blk}, T_{op}) = \max\left(i_{II}(t), t \in [T_F, T_{backup}]\right)$$

The total fault neutralization time for backup protection is at least twice as long as primary protection but obviously the increase of fault current in adjacent branches is lower compared to the faulted branch itself. Before defining a specific STB for CBC determination in case of backup protection a sensitivity analysis is carried out to verify if CBC requirements can be higher compared to primary protection requirements. The test grid is shown in Figure 122. The test grid consists of two adjacent nodes to consider fault current contributions from potential future grid extensions.

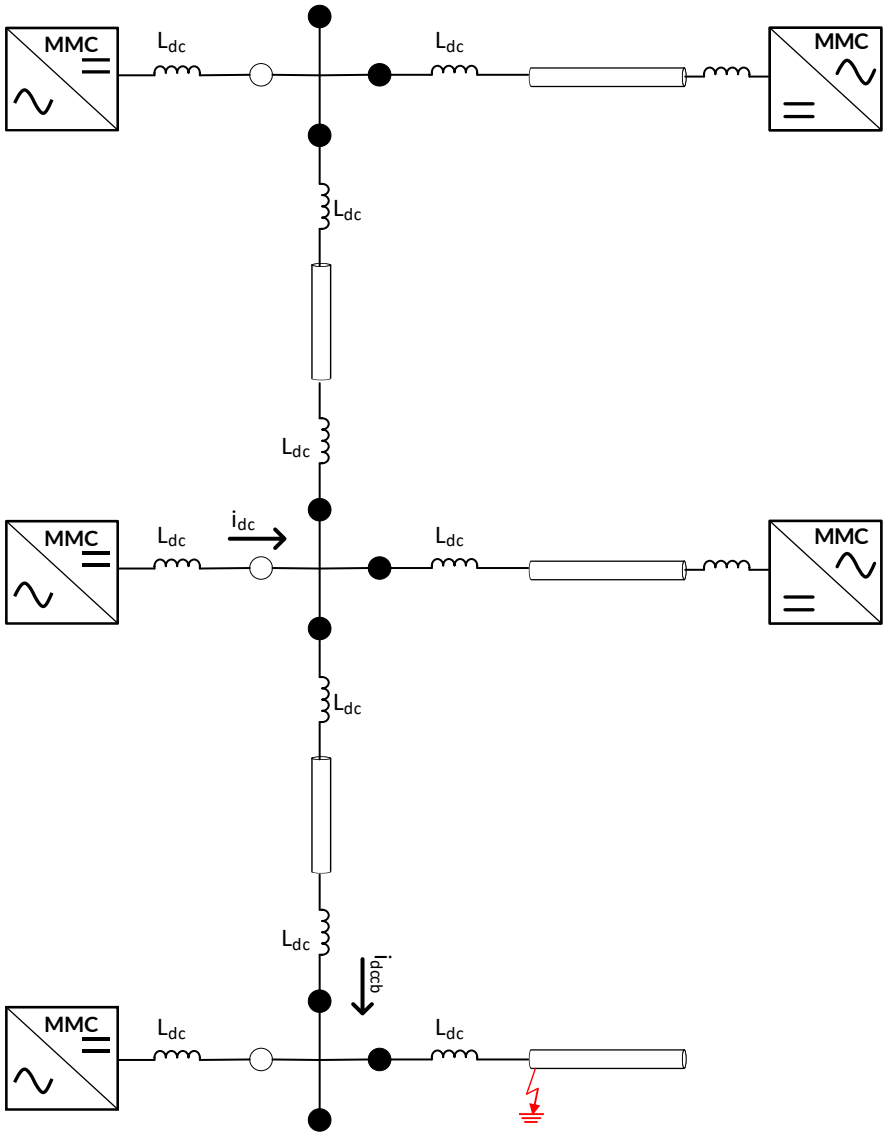


Figure 122 Extended test grid to compare CBC requirements during backup protection with primary protection: Spoke fault with breaker failure at spoke

7.5.3. Results

The current breaking capability requirements for DCCBs at spoke and interconnectors are shown in Figure 123. It should be noted that the results consider the required DCCB operating time to respect the blocking constraints as shown in Figure 118. A first conclusion that accounts for all curves is that an increasing DC reactor does not lead to a lower current breaking capability requirement. In fact, the curve is either flat or slightly increasing ($i_{dc,blk}$=5pu). This underlines that the highest design constraint is imposed by the DC current blocking criteria and the dedicated time to block. The DC reactor is a mean to increase this time but since the maximum MMC current level will be the same for all DC reactors the CBC does not increase. Secondly, it can be observed that an increase of MMC DC current blocking criteria leads to an increase of CBC requirement. The increase of 1pu of $i_{dc,blk}$ leads to an increase of about 3.1kA for the current breaking capability. It should

further be noted that the curves show only the results that are feasible in terms of DCCB operating times (T_{op}>0s).

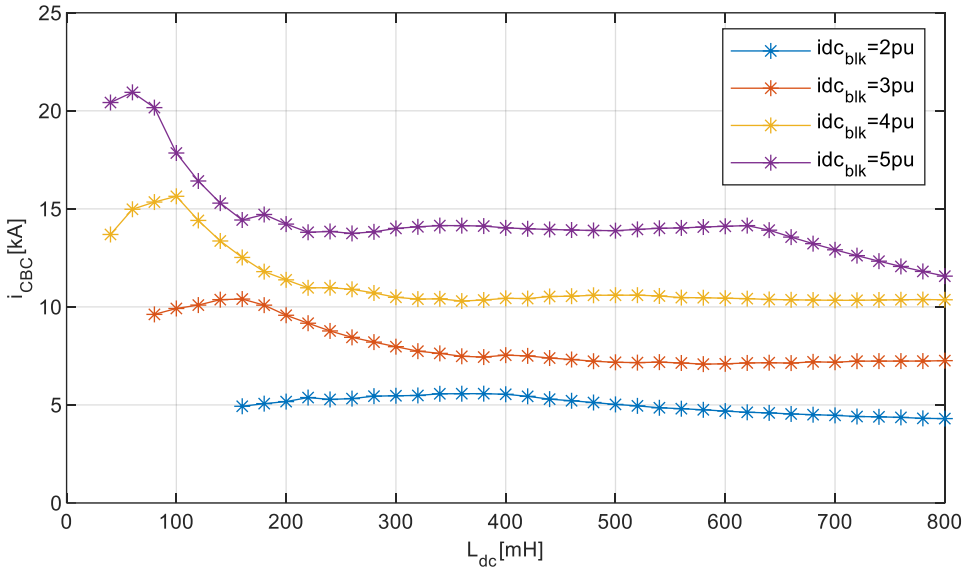


Figure 123 Current breaking capability requirements for DCCBs at spoke and interconnectors in dependence of DC reactor and MMC DC current blocking criteria; T_{BFI}=1ms, T_{relay}=0.5ms

The current breaking capability of the DCCB at the onshore converter needs to be such that the DC current blocking criteria of the onshore converter is respected. (e.g. I_{CBC}=10kA for $i_{dc,blk}$=5 pu).

Figure 124 compares the CBC requirements for primary protection with the CBC requirements for backup protection (see topology Figure 122). The backup protection requirements are lower for all combinations of $i_{dc,blk}$ and L_{dc}. The same conclusion can be drawn for a breaker failure identification time of 3ms (see Appendix 12.3). Hence the CBC for this 4-feeder configuration can be purely determined by the primary protection STB (see Figure 121).

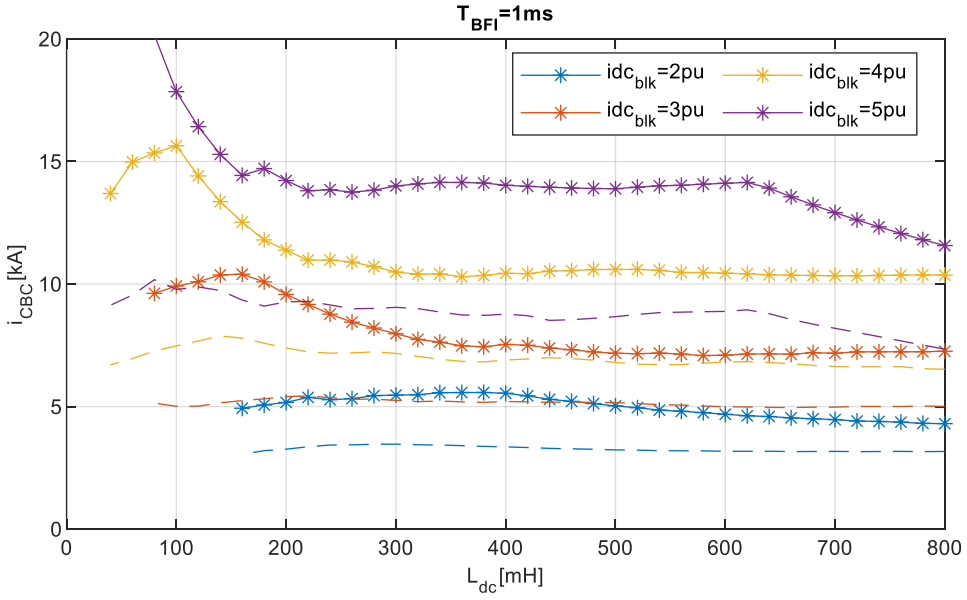


Figure 124 Comparison between CBC requirements for primary protection (solid) and backup protection (dashed); T_{BFI}=1ms

The results from previous sections can be used to narrow down the parameter ranges for the operating time, the current breaking capability, dedicated DC reactor requirements and reasonable DC current blocking criteria.

Figure 125 links the results of Figure 118 and Figure 123 such that possible combinations of DC reactor requirements, operating times and current breaking capabilities can be found in a single figure. The left axis indicates the current breaking capability and is linked with 'star lines' (*). The right axis indicates the DC reactor value and is linked with 'dotted lines' (•). Both are shown in dependency of the operating time T_{op}. The colors indicate the DC current blocking criteria. It is clearly visible that an increase of operating time leads to a quasi-linear increase of DC reactor requirements while the current breaking capability remains rather unchanged.

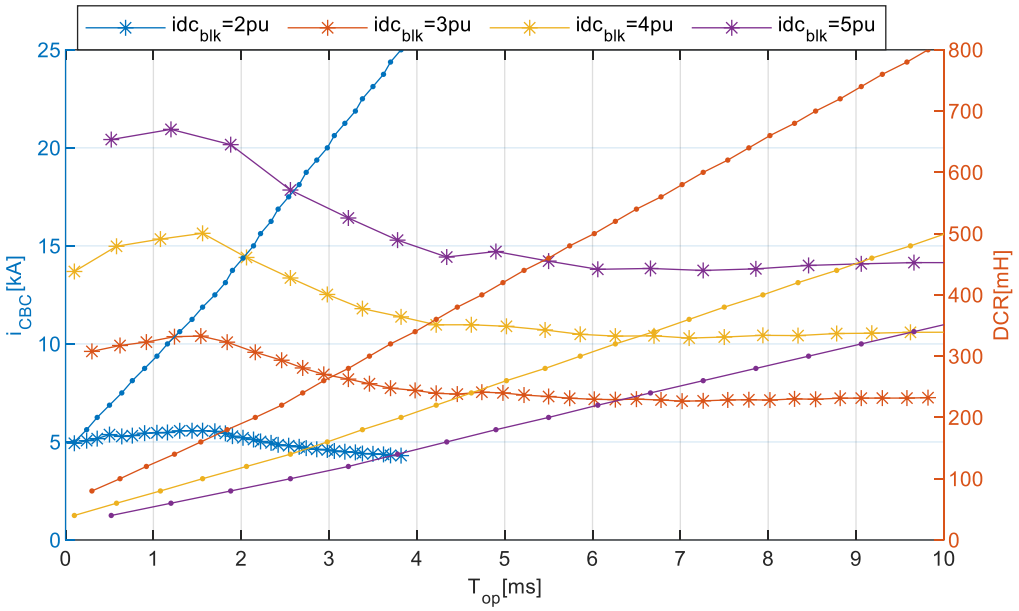


Figure 125 Current breaking capability (left axis) and DC reactor requirements (right axis) in dependence of DCCB operating time; T_{BFI}=1ms, T_{relay}=0.5ms. The left and right axis are linked respectively with 'star lines' (*) and 'dotted lines' (•)

The results from previous sections can be used to narrow down the parameter ranges for the operating time, the current breaking capability, dedicated DC reactor requirements and reasonable DC current blocking criteria. The consequent number of possible combinations are synthesized in Table 38 in order to show possible combinations for DCCB operating times T_{op}={1.5; 3; 5; 10}ms. This can be used as tendering material parameter range specifications.

Successful laboratory demonstrations show that operating times of 1.5ms are achievable [27]. High operating times (i.e., above 10ms) lead to high values of DC reactors and could impact the response time of the grid as well as the controllability. The upper limit of acceptable DC reactor values should be coordinated with converter control aspects and response time requirements (see section 6.3.3).

It should be noted that the results are minimum requirements considering the fault identification time T_{relay}=0.5ms and the breaker failure identification time T_{BFI}=1ms. Safety margins can be added to the defined values. A sensitivity analysis according to variation of T_{relay} and T_{BFI} is provided in appendix 12.1. As mentioned in section 7.2 the DC current blocking criteria of 3pu is largely compatible with IGBT current limits of 2pu. Hence, the lower parameter range limit is set to $i_{dc,blk}$=3pu.

Table 51 DCCB and DCR specifications for different DCCB operating times; T_{BFI}=1ms, T_{relay}=0.5ms

DCCB operating time	I_{dcblk}=2pu		I_{dcblk}=3pu		I_{dcblk}=4pu		I_{dcblk}=5pu	
	L_{dc} [mH]	i_{CBC} [kA]	L_{dc} [mH]	i_{CBC} [kA]	L_{dc} [mH]	i_{CBC} [kA]	L_{dc} [mH]	i_{CBC} [kA]
1.5ms	380	6	160	11	100	16	80	15
3ms	660	5	280	9	180	12	120	15
5ms	>800	5	440	8	260	11	200	17
10ms	>800	5	>800	8	500	11	360	21

7.5.4. Conclusions

Table 52 Functional requirements related to DCCB current breaking capability

ID	Functional requirement
General77	The current breaking capability of the DCCB should be sufficient to interrupt fault currents during primary and backup protection sequences.

Table 53 Parameters related to DCCB current breaking capability

ID	Symbol	Characteristic/Events	Range
108	i_CBC	DCCB current breaking capability	[5-21] kA

7.6. DCCB energy absorption and fault current suppression time specifications

7.6.1. Methodology

From fault neutralization to current zero the DC circuit breaker absorbs the magnetic energy of the fault current stored in the DC reactors. This section intends to specify the parameter range of the surge arrester energy absorption requirements as a function of the chosen DC reactor value and the authorized DC current blocking criteria. The simplistic test benchmark is introduced in the following section and will be tested against the use cases 1.1 and 1.2 for a number of feasible combinations of DC reactors, DCCB operating times and DC current blocking criteria is used (results from section 7.3 and 7.5, see Table 54). Energy absorption requirements and the fault current suppression time (time from fault neutralization to current zero) will be specified based on the test scenarios.

Table 54 Test scenarios for energy absorption requirement and fault current suppression time specifications

T_op [ms]	DCR [mH]		
	$I_{dc,blk}$=3pu	i_{dc_blk}=4pu	i_{dc_blk}=5pu
2	200	120	100
4	360	220	160
6	500	320	220
8	660	420	300
10	800	500	360

7.6.2. Simplistic test benchmark

Figure 137 shows the STB that is used to estimate the surge arrester energy absorption requirements as well as the time from fault neutralization to current zero. The STB represents the MMC connected to the node as well as two feeders represented by ideal voltage sources. It should be noted that only DC reactors connected to the node are represented. The simplified DC circuit breaker model as introduced in section 5.5 is used.

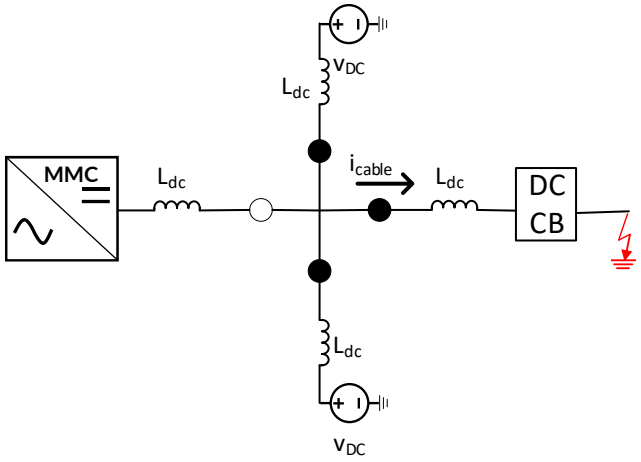


Figure 126 STB for energy absorption specification

7.6.3. Results

The results for the DCCB energy absorption requirements related to a single operation of the DCCB for the test scenarios are shown in Figure 127 and are compared against use case results. The fault in use case 1.1 is located at spoke L2 (one interconnector), whereas in use case 1.2 the fault is applied at spoke L1 (2 interconnectors). It should be noted that the energy absorption requirements need to be doubled in case of an OCO. The following observation can be made:

- → The energy absorption requirements are approximately linearly dependent on the DC reactor value L_{dc}.
- → The energy absorption requirement increases importantly with increasing DC current blocking criteria and hence higher fault current to be interrupted.
- → The STB provides a conservative approximation of DCCB energy absorption. The values of the STBs are superior to the actual values from the use cases. The gap increases with increasing DC reactor values and operating times. The difference can be explained by the simplified approach of interconnector representation. Ideal voltage sources provide a conservative estimation of the rise of fault current. As the magnetic energy is proportional to the square of the fault current it is rather logical that the energy absorption is overestimated.
- → An increase of the number of interconnectors from one in use case 1.1 to two in use case 2.2 leads to an increase of energy absorption

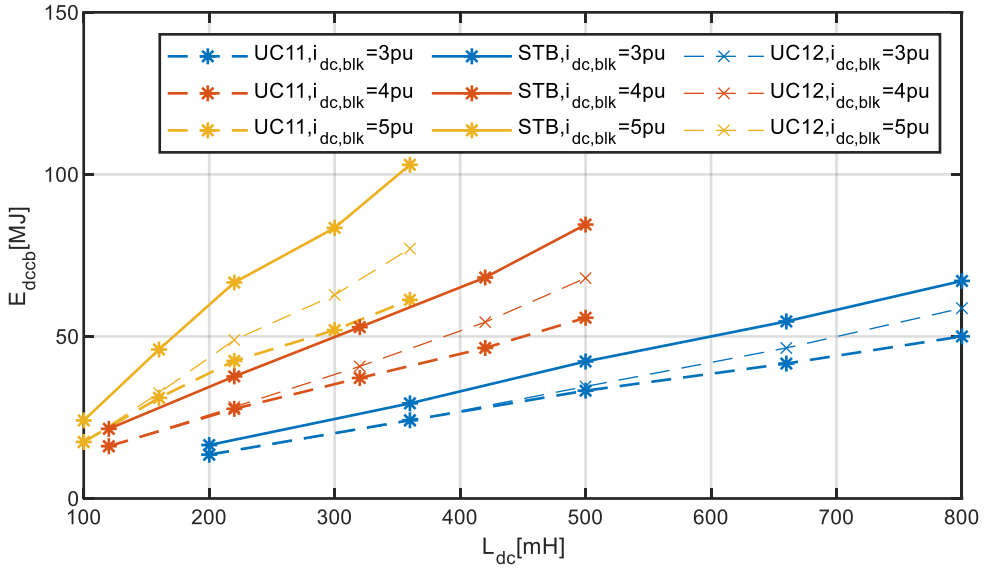


Figure 127 DCCB energy absorption requirements for fault current suppression at spoke for the combination of test cases; STB results (solid), Use case 1.1 results (dashed*), Use case 1.2 results (dashed^x)*

Figure 128 shows the fault current suppression time T_{zero} for the test cases compared to use case 1.1 and 1.2. The following observations can be made:

- → Fault current suppression time is linearly dependent on the DC reactor size
- → For an identical DC reactor the fault current suppression time increases with increasing DC current blocking criteria
- → For the given test cases an overall range between 7ms and 36ms can be identified

The fault current suppression time is of particular interest when it comes to overvoltage ride through of converters. In fact, during fault current suppression the TIV of the DCCB is imposed to other elements of the grid. The converter needs to operate during fault current suppression time and should remain stable despite of the important overvoltage at the output.

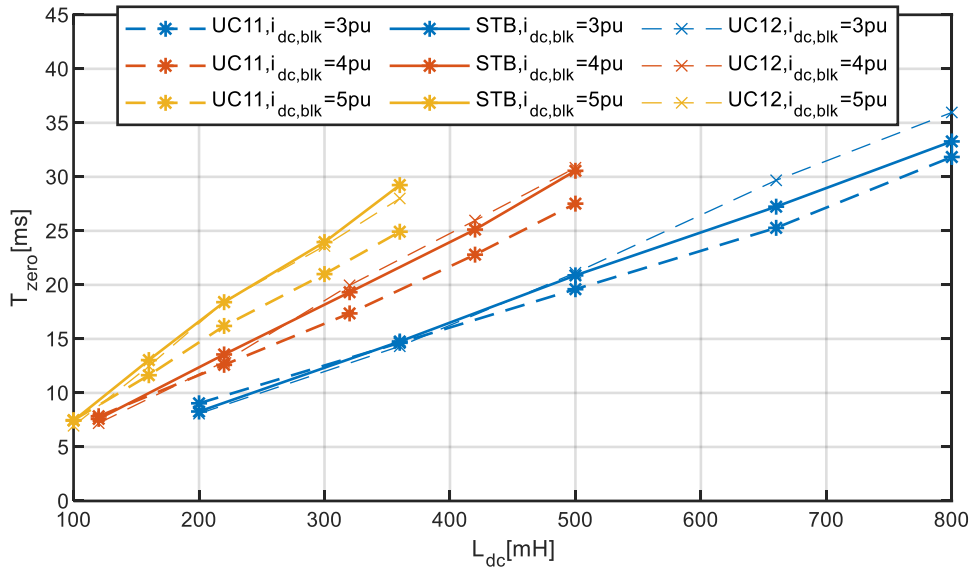


Figure 128 Fault current suppression time requirements for fault current suppression at spoke for the combination of test cases; STB results (simplistic), Use case 1.1 results (dashed), Use case 1.2 results (dashed^x)*

7.6.4. Conclusions

Table 55 Functional requirements related to DCCB energy absorption and fault current suppression time

ID	Functional requirement
General75	The fault current suppression time should be specified such that all grid components support the temporary overvoltage and current dynamics during this process.
General76	The transient interruption voltage (TIV) during the fault current suppression process of the DCCB should be designed taking into account constraints coming from insulation coordination design and should be coordinated with the pole-to-ground arrester clamping voltage.

Table 56 Parameters related to DCCB energy absorption and fault current suppression time

ID	Symbol	Characteristic/Events	Range
128	E_DBS	DBS Energy dissipation capacity (single opening sequence[14])	[40-250] MJ
129	T_zero	Fault current suppression time	[1-50] ms
130	U_TIV	DCCB Transient interruption voltage	[1,5-1,7] pu

[14] Note that the given energy absorption values correspond to a single DCCB operation. If a second opening sequence is required (i.e. after reclosing) this number should be doubled

7.7. DBS activation specifications

7.7.1. Methodology

The dimensioning scenarios for DC side overvoltage specifications related to Dynamic Braking System (DBS) activation are listed in Table 57. The onshore converter blocking scenario and spoke fault scenario are investigated in the use case PSCAD environment since the activation of the DBS provokes high switching transients. Within this study, only DBS at the DC side is investigated. Note that for the definition of functional requirements and parameter range for DBS the use case 1.1 has been considered. Regarding the DBS model, it has been received as input for this study. It includes a resistor in series with a switch where its duty cycle is adjusted based on a simple DC overvoltage control. More information can be found in [28]

Table 57 Dimensioning scenarios for temporary overvoltage due to DBS operation

Scenario	Description	Estimated time
Onshore converter blocking	A blocking of an onshore converter in inverter mode leads to a power flow imbalance. The temporary surplus of power needs to be shifted to remaining available converters which leads to a temporary overvoltage. Two cases must be considered: - Remaining converters have sufficient headroom to handle new load flow such that DBS operation and WF ramp-down is not required - The remaining converters do not have sufficient headroom to handle new load flow: DBS must be activated and WFs must be ramped down.	Several seconds (depending on DBS activation time and WF ramp down rate
Spoke fault	Similar to 'Onshore converter blocking' but the DBS at the onshore converter which is out of operation is not available for energy dissipation. Hence, this is the dimensioning scenario as it leads to the lowest number of DBS available	Several seconds (depending on DBS activation time and WF ramp down rate

An important parameter to be investigated in this context is the DBS overvoltage activation limit. In Point-to-Point connections, the overvoltage limit of the DBS is simply chosen such that overvoltage at the inverter station is avoided. If the inverter station is not available (due to blocking or AC faults) the DBS allows to dissipate the energy surplus until wind farms are ramped down or disconnected. Hence, it can be assumed that local information can be exchanged between converter and DBS. In MTDC grids however, a spoke fault leads to a surplus of energy at other inverter stations and the DBS is a mean to keep the remaining grid operational. It is further possible that several DBS are activated simultaneously where autonomous activation based on local measurements is required. The time frame for the DBS activation is from spoke disconnection to WF ramp-down. Two cases are possible:

→ The onshore converters have sufficient headroom to handle the new load flow without DBS activation and without WF ramp-down

→ DBS must be activated to absorb the surplus of energy (full load as worst case)

Regarding the first case, the question arises if dynamic activation of the DBS should be transiently allowed even though the load flow could be handled without activation. The consequences of the choice of DBS activation threshold on overvoltage in MTDC grids will be discussed in the following section.

7.7.2. Results

According to the methodology in section 7.7.1 the dimensioning scenario for temporary overvoltage is the spoke fault. Four test scenarios as listed in Table 58 will be investigated in this section. In the first two test scenarios a low DBS voltage threshold is chosen (1.07pu), whereas in Test scenarios 3 and 4 the threshold is set to 1.2pu. This allows to investigate the impact of a dynamic DBS activation even if the new load flow is not exceeding the remaining converter limits.

Table 58 DBS test scenarios

DBS simulation cases (Fault type: spoke)	**DBS DC voltage limit [pu]**	**Load flow**
Test scenario 1	1.07	Not exceeding
Test scenario 2	1.07	Exceeding
Test scenario 3	1.2	Not exceeding
Test scenario 4	1.2	Exceeding

Figure 129 shows the results for the four DBS test scenarios from fault inception at T=0s to ramp-down of WF at about 2.9s. The ramp-down of the WF for Test scenario 2 and 4 starts at T=0.4s. For test scenario 1 et 3 the simulation stops at T=0.9s since WF ramp-down is not necessary. The results show that if the DBS voltage activation limit is chosen at 1.07 this results in a temporary DBS activation even though it was not strictly necessary when considering the load flow (Test scenario 1). If a higher threshold is chosen (1.2 pu) the temporary (and unnecessary) DBS activation can be avoided (Test scenario 3). However, if DBS activation is required and a high DBS activation threshold is chosen (Test scenario 4) the onshore converter is constantly regulated to 1.2pu which leads to an overvoltage in the whole system of about 1.25pu for several seconds. Secondly, DBS activation at a higher overvoltage level also leads higher voltage dynamics at offshore converters (maximum value for MMC2-2 is 1.32pu).

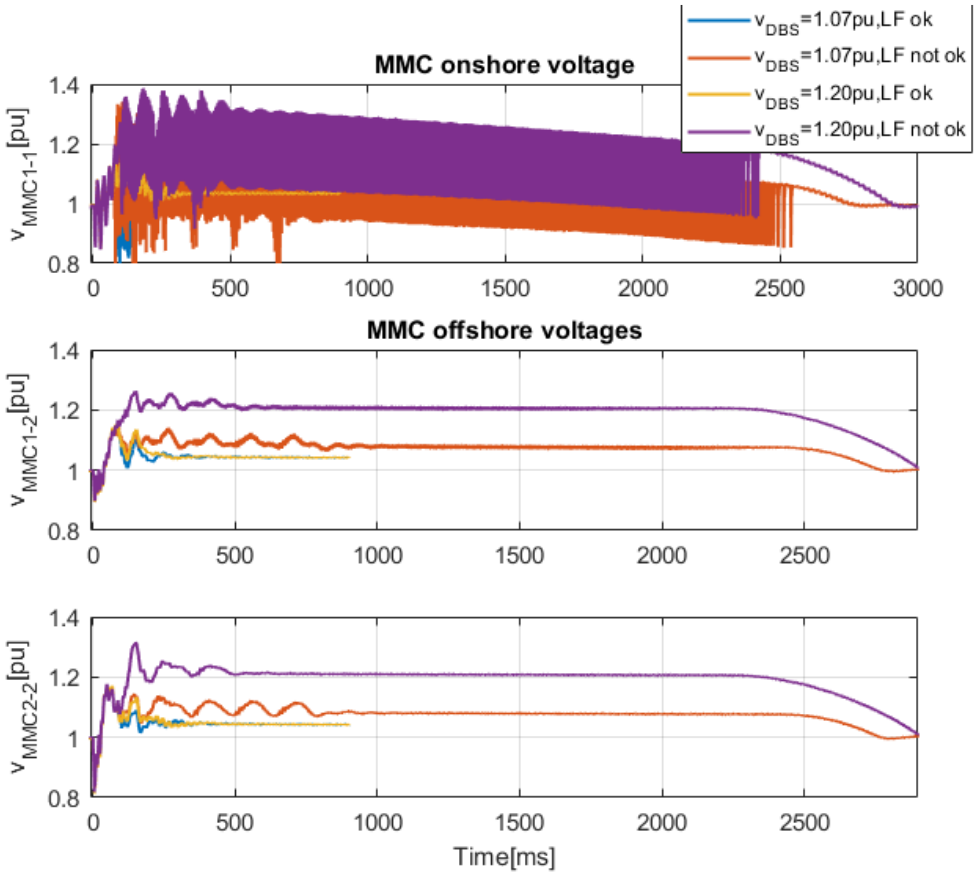


Figure 129 Voltage profiles for onshore and offshore converters for DBS test scenarios

7.7.3. Conclusions

It can be concluded that the DBS voltage activation level is mainly influencing the overvoltage that needs to be sustained by all converters until appropriate WF ramp-down which can take several seconds. The DBS voltage activation threshold should be compliant with converter overvoltage capabilities such that controllability during WF ramp-down is ensured.

The activation and control of the DBS should be done locally at the substation. This is mainly due to the fact that voltage increases fast in a range of several milliseconds. With local coordination additional communication delay can be avoided. However, this should be subject to a broader coordination study.

The results also showed that an overvoltage activation threshold is not straightforward to determine. In fact, if a low overvoltage activation threshold is chosen the DBS risks to be operated transiently even though converter could have managed the power transfer independently. On the other hand, if the overvoltage activation threshold is chosen to be high, the simulation results showed that all converters in the grid must operate at a high voltage level for several seconds.

Considering this, an advanced functional requirement of active voltage ramp down by the DBS as schematically shown in Figure 139 could be an alternative. In this way, the overvoltage activation threshold could be chosen such that DBS is only activated if strictly necessary by choosing a sufficiently high threshold v_{DBS}. At T_{ON2} the WF ramp-down starts. The standard solution keeps operating at the DBS overvoltage activation threshold v_{DBS} whereas the advanced solution keeps the operation at P_{DBS}=1pu until the voltage is reduced close to the rated

value. This allows to operate at a reduced voltage level compared to the standard solution until WF ramp-down stops. The total duration of DBS operation T_{DBS} for both solutions is determined by the ramp-down time of the wind farms $T_{WF,RD}$ plus ramp-down activation time T_{ON2}.

$$T_{DBS} = T_{WF,RD} + T_{ON2}$$

The required minimum energy dissipation level for the DBS is obtained by the following equation considering that the maximum power to be dissipated is the rated power of one converter P_{MMC}.

$$E_{DBS} = \int_0^{T_{DBS}} P_{DBS}\, dt = P_{MMC}\left(\frac{T_{WF,RD}}{2} + T_{ON2}\right)$$

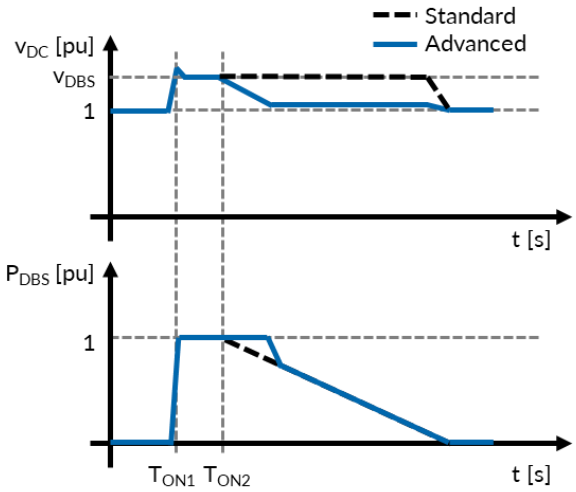


Figure 130 Schematic voltage and power curve for DBS with advanced control functions; comparison between standard and advanced DBS functions

Such additional functional requirements of DBS can improve the performance during DC grid contingencies. However, possible control interactions between converters, DBS and wind farms must be thoroughly investigated.

Figure 131 gives an overview on the DBS energy absorption requirement for P_{MMC}=1GW depending on wind farm ramp-down rate p_{WF} and ramp-down activation time T_{on2}.

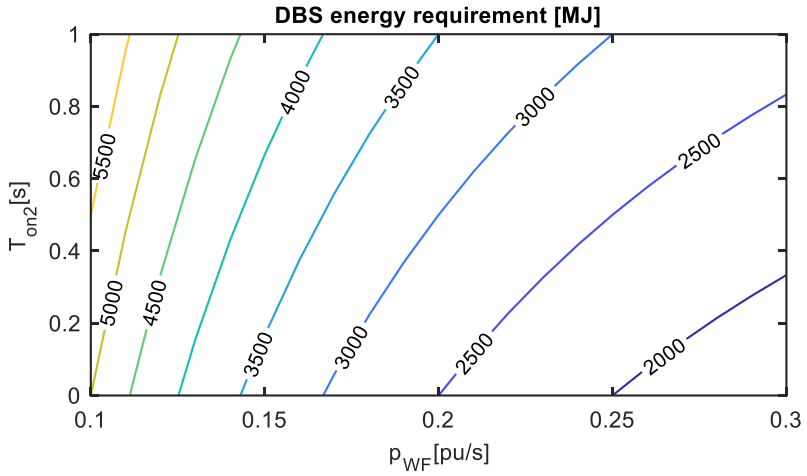


Figure 131 Overview of DBS energy absorption requirement E_{DBS} for P_{MMC}=1GW depending on wind farm ramp-down rate p_{WF} and ramp-down activation time T_{on2}

Table 59 Functional requirements related to DBS activation

ID	Functional requirement
General54	The DC system or each specific protection zone should be equipped with sufficient energy dissipation devices (i.e. DBS) in case of power imbalance. The parameters of the energy dissipation devices should be specified in the dedicated building block (i.e. converter unit and/or switching station)
General73	The DBS should limit the overvoltage to an acceptable voltage level such that controllability of converters is ensured and should be activated sufficiently fast to avoid exceeding the voltage level
General74	The DBS should dissipate the energy surplus during the ramp-down process of the wind farms

Table 60 Parameters related to DBS activation

ID	Symbol	Characteristic/Events	Range
126	U_DBS	DBS should be activated when overvoltage level is exceeded	[1,05-1,2] pu
127	t_DBS	Activation time after overvoltage threshold is exceeded	
128	E_DBS	Energy dissipation requirement of DBS	[1600-6000] MJ

7.8. Validation with Use cases

In the previous section generic results have been provided for a 4-feeder hub as shown in Figure 112. The results consist of combinations of DC reactors, DC blocking current, DCCB operating time, current breaking capability, DCCB energy absorption requirements and fault current suppression time. In this section, a selection of protection equipment parameters is tested against the three use cases shown in Figure 132 using simplistic model proposed in section 5. The STB validation against uses cases using more detailed PSCAD model is shown in appendix 12.4. The fault is applied on spoke L2 (0km, 200km, 400km distance from Bb2). The selection is listed in Table 61. It covers a DCCB operating range from 2-10ms and a DC current blocking criteria from 3-5pu. Relay time and breaker failure identification time are set to 0.5ms and 1ms respectively.

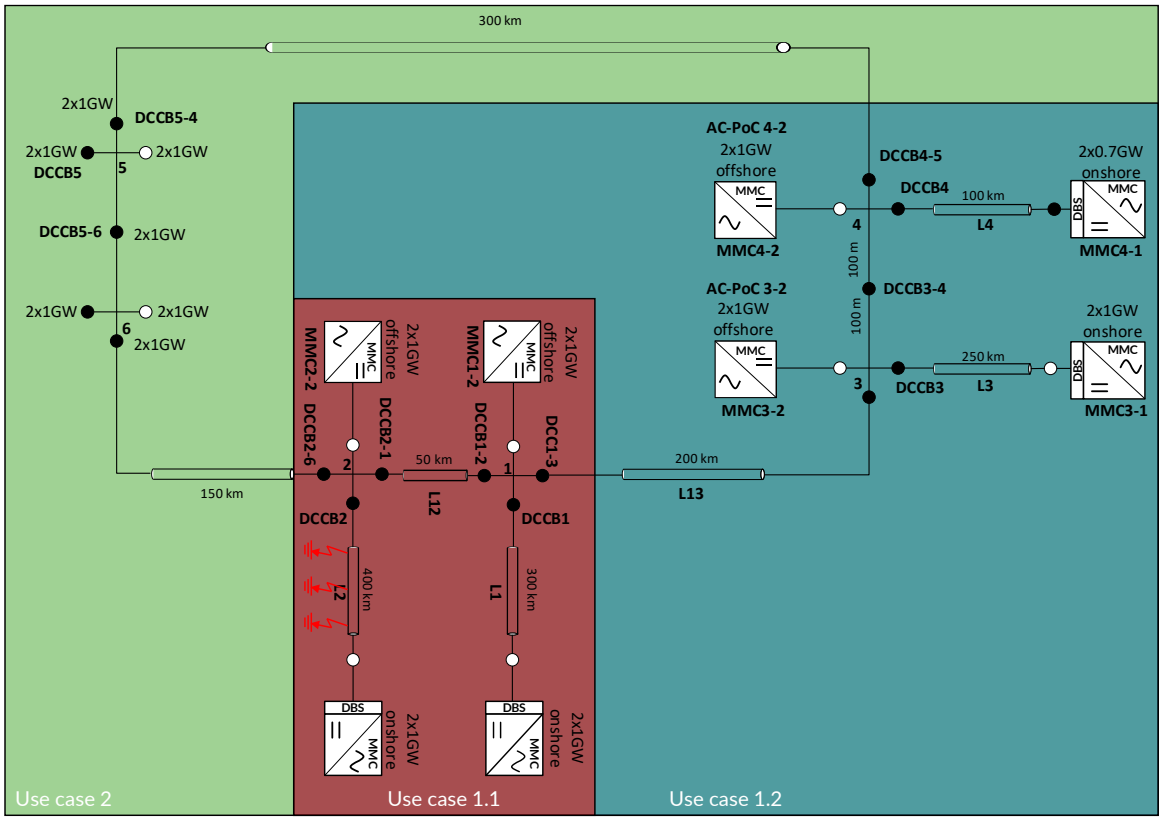


Figure 132 Use case test topologies for protection parameter validation

Table 61 Selection of use case 1.1 test parameters according to results in section 7.3

T_op [ms]	idc_blk=3pu	idc_blk=4pu	idc_blk=5pu
	Ldc [mH]		
2	200	120	100
4	360	220	160
6	500	320	220
8	660	420	300
10	800	500	360

The worst-case primary protection scenario is a spoke fault with opening of the dedicated DCCB2. The protection sequence is as follows:

1. Fault inception at spoke L2
2. Fault clearing by opening DCCB2
3. Activation of DBS at MMC1-1 if power cannot be evacuated (v_{DBS}=1.2pu)
4. Ramp-down of WF

The worst-case backup protection scenario is a spoke fault with breaker failure and backup protection by adjacent DCCBs, in this case the opening of DCCB2-1. The backup protection sequence is as follows:

1. Fault inception at spoke L2
2. DCCB2 fails to open
3. DCCB2-1 opens
4. New load flow in remaining system (MMC1-2 and MMC1-1)

In total, a number of 45 use case simulations are carried out for each use case:

- → Iteration of fault location on spoke L2: 0km – 200km – 400km from Bb2
- → Iteration of protection equipment (see Table 61)

For each simulation, the following quantities are verified, and the maximum value is retained:

- → Respect blocking conditions of converters
- → Respect of current breaking capability of DCCB within the specified time
- → Respect of DCCB energy absorption requirements
- → Respect of DCCB fault current suppression time

7.8.1. Primary protection

The results for the maximum fault current contribution from MMC 2-2 and maximum current breaking capability for fault current interruption at the spoke are respectively shown by the solid lines in the top and bottom graphs of Figure 133. The dashed lines indicate respectively the DC current blocking criterion and the current breaking capability obtained from the STB in section 7.5. The following observation can be made:

→ DC current blocking criterion

> For all simulations the converter currents remain below the DC current blocking criterion which shows that the blocking criterion is respected and well dimensioned.

> Use case 1.1 and 1.2 lead to almost identical maximum converter currents. This leads to the conclusion that grid extensions at other hubs (in this case Bb1) has very limited impact on the design of the actual hub (in this case Bb2). However, adding an interconnector to Bb2 (Use case 2) lowers the maximum converter current contribution for a spoke fault.

> As expected, the dimensioning scenario to respect he DC current blocking criterion of the converter is the case with a single feeder (Use case 1.1 & 1.2)

→ Current breaking capability for DCCB at spoke

> The current breaking capability resulting from the STB is not exceeded for all simulation cases.

> The current breaking capability requirements increase for Use case 2. The second interconnector leads to higher fault current contribution due to more capacitive discharge from the second interconnector. It can be seen that Use case 2 results approach the current breaking capability estimation by the STB model (dashed lines).

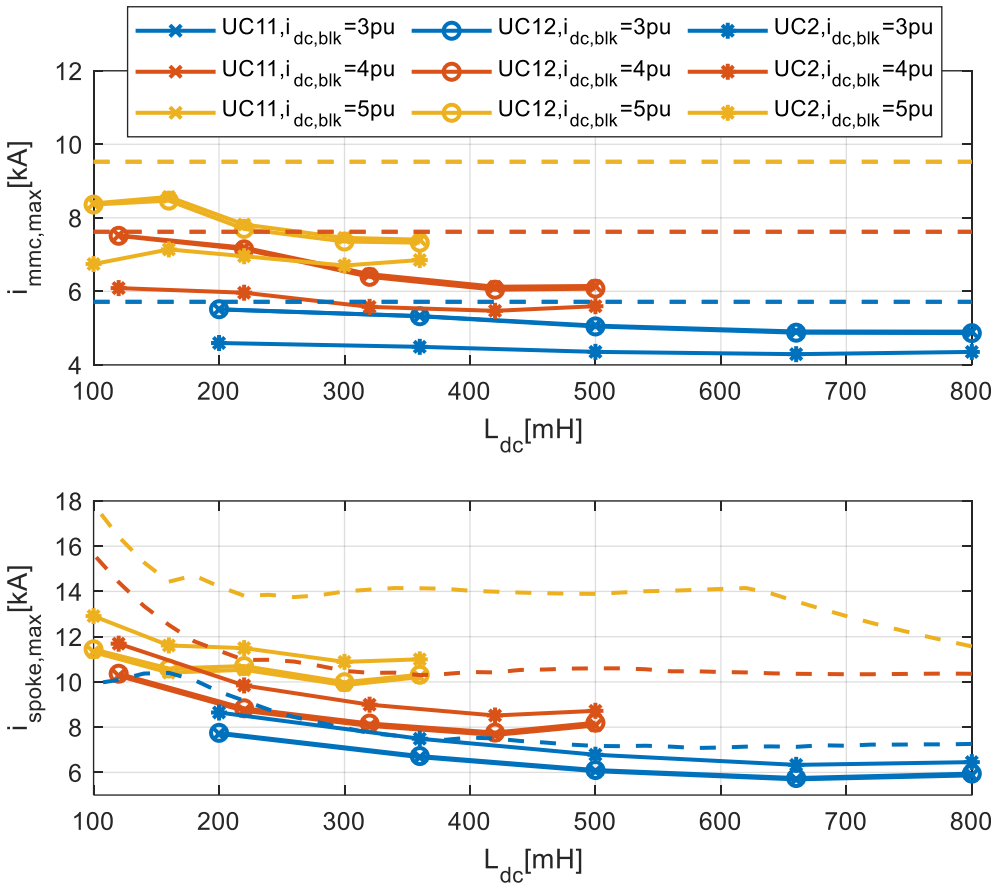


Figure 133 Results for Use Cases: current contribution from MMC 2-2 and maximum current to be cleared by DCCB2. Dashed lines indicate respectively the DC current blocking criterion and the current breaking capability defined by means of STB

The margins between the results from the STB and the use case simulations are listed in Table 62. The margins have been calculated based on the following equations:

$$\Delta i_{mmc} = i_{dcblk} - i_{mmc,max}$$

$$\Delta i_{CBC} = i_{CBC} - i_{spoke,max}$$

Table 62 Margin between STB results and use case results for current breaking capability and DC current blocking criterion; margin provided in kA

	Current breaking capability margin Δi_{mmc}				DC current blocking criterion Δi_{CBC}		
		i_dcblk[pu]			i_dcblk[pu]		
UC 1.1	**T_op [ms]**	**3**	**4**	**5**	**3**	**4**	**5**
	2	1,9	4,1	6,5	0,2	0,1	1,1
	4	0,8	2,2	4,0	0,4	0,4	1,0
	6	1,1	2,3	3,3	0,6	1,2	1,7
	8	1,4	2,8	4,1	0,8	1,5	2,1
	10	1,4	2,5	3,9	0,8	1,5	2,1
		i_dcblk[pu]			i_dcblk[pu]		
UC 1.2	**T_op [ms]**	**3**	**4**	**5**	**3**	**4**	**5**
	2	1,8	4,0	6,4	0,2	0,1	1,2
	4	0,8	2,1	3,8	0,4	0,5	1,1
	6	1,1	2,2	3,1	0,7	1,2	1,8
	8	1,4	2,7	4,0	0,8	1,6	2,2
	10	1,3	2,4	3,8	0,9	1,5	2,2
		i_dcblk[pu]			i_dcblk[pu]		
UC 2	**T_op [ms]**	**3**	**4**	**5**	**3**	**4**	**5**
	2	0,9	2,7	4,9	1,1	1,5	2,8
	4	0,0	1,1	2,8	1,2	1,7	2,4
	6	0,4	1,4	2,3	1,4	2,0	2,6
	8	0,8	1,9	3,1	1,4	2,2	2,8
	10	0,8	1,9	3,1	1,4	2,0	2,7

Figure 134 shows the results for maximum DCCB energy dissipation and fault current interruption time in top and bottom graph respectively. The use case results confirm that DCCB energy dissipation and fault interruption time increase with increasing operating time and DC current blocking criterion. Use case 1.1 is the dimensioning case as it provokes the highest energy to be absorbed and the highest fault current interruption time compared to other use cases.

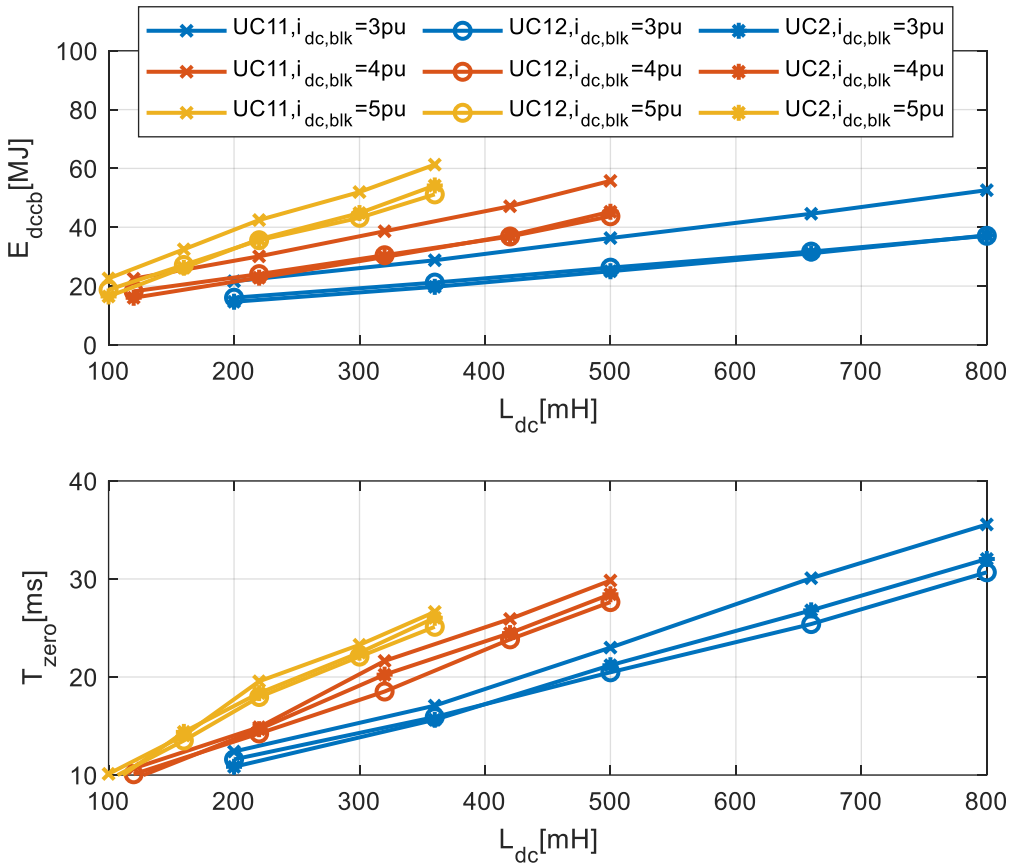


Figure 134 Results for *Use cases: Maximum DCCB energy dissipation (top) and maximum fault current interruption time (bottom)*

8. Functional group – DC ancillary services

Disclaimer: Reference documents such as [29] and CENELEC standards typically refer to DC "ancillary services". This wording is kept here but it does not convey any statement about which functionality shall be provided through market or not.

According to [29], DC equipment can provide ancillary services for the HVDC grid itself. Such ancillary services are

- → DC energy balance and reserve
- → DC transmission capacity reserve and power flow control
- → DC transmission loss compensation
- → Energizing of DC subsystems, DC black start and restoration

The second and third, in our understanding, boils down to the availability and use of an optimal power flow controller for the combined AC and DC grids, which is considered beyond the scope of the study. The first and last services are further detailed.

The HVDC system can also provide ancillary services for the AC system [3], [30]. This type of ancillary services from HVDC to AC system is addressed within SoW A.

8.1. DC Energy balance and reserve

The stability of the DC grid relies on the balance between input and output power. Any fluctuation must be compensated, based on control mechanisms such as

- → DC node voltage control
- → Coordinated system control

The power reserve available to those controllers can be defined as ancillary services. The presence of a Dynamic Braking System (DBS) can thus be seen as an ancillary service and is addressed in Section 7.6.

8.2. Energizing of DC subsystems, DC black start and restoration

DC black start is addressed as a specific start-up sequence in Section 9.2.6.

8.2.1. Methodology

The energization of DC subsystems includes the energization of

- → Converter stations in blocked state
- → Deblocking and energization of converter stations
- → Cables

The energization of converter stations in blocked state is addressed in Section 8.3. The deblocking of a partially charged converter station is typically done during start-up and is addressed in the corresponding section under

Operational Regimes. The energization of cables independently from the start-up procedure is addressed in this section.

The cables can be energized from any available part of the DC grid. We consider the general case where a cable is energized from a DC grid comprising at least one onshore converter station. The considered energization process comprises the closing of the PIR on one side of the cable only. The other side of the cable remains open until the voltage is stabilized around the nominal value. Once the cable has been energized from one side, the closing at the other end of the cable thus does not induce any significant voltage surge as both sides are around the nominal voltage. Only the first closing onto the PIR is thus further investigated.

During the energization, a current surge will occur, associated to both overvoltages and undervoltage. This current surge may exceed the overcurrent capability of a converter station. To avoid this, a pre-insertion resistor can be used, in association with the closing breaker/switch, to add a resistance in the current path and limit the overcurrent.

The following elements are expected to affect the dynamic response of the energization

- Topology of the network: number of connected cables/stations
- Length of the cables
- Size and location of the inductors
- Parameters dimensioning the PIR

The main dimensioning parameters of the PIR are

- Resistor value
- Electrical Insertion Time (EIT): time interval during which the PIR is inserted
- Energy dissipation capability

Finally, the main performance indicators are

- Overcurrent at the output of the converter station(s)
- Overvoltage at the opened remote end of the cable
- Undervoltage at the PoC-DC

While various energization cases can be considered, we will focus on dimensioning scenario. The maximum overcurrent at the output of an MMC will correspond to the case where the cable is charged from a single MMC, without any adjacent cables. In any other situations, the current going into the cable will be split into several source, including converters and cables. Thus, the dimensioning scenario consists of the energization of cable connected only to an onshore converter station. This is also a conservative scenario as there is only one inductor, assumed at the output of the converter, between the converter and the cable.

8.2.2. STB: Simplified cable energization

The proposed Simplistic Test Benchmark to represent the dimensioning scenario comprises the AVM model DC for the converter and the Pi model for the cable, as depicted in Figure 135: STB for PIR sizing. The voltage source can be disconnected to account for the capacitive discharge only. The overcurrent is measured at the output of the MMC. The voltages are measured at both ends of the cable. In practice, undervoltage will be critical at the closing end (left side) while the overvoltage will be considered at the open end (right side), as high overvoltage can be expected due to the traveling wave phenomenon. In a worst-case approach, no surge arresters are considered at the ends of the cable in the STB.

Two variants of the AVM DC model presented in Figure 27 are considered

- An RLC circuit with charge capacitor at the nominal voltage. The parallel current source is set to 0 as no power flow can be applied before the energization of the cable. This model will only represent the discharge of the converter submodule in the cable.
- An RL circuit with ideal voltage source, to account for the voltage control of the converter. This can be seen as a worst-case control scheme with the ability to perfectly control the converter voltage.

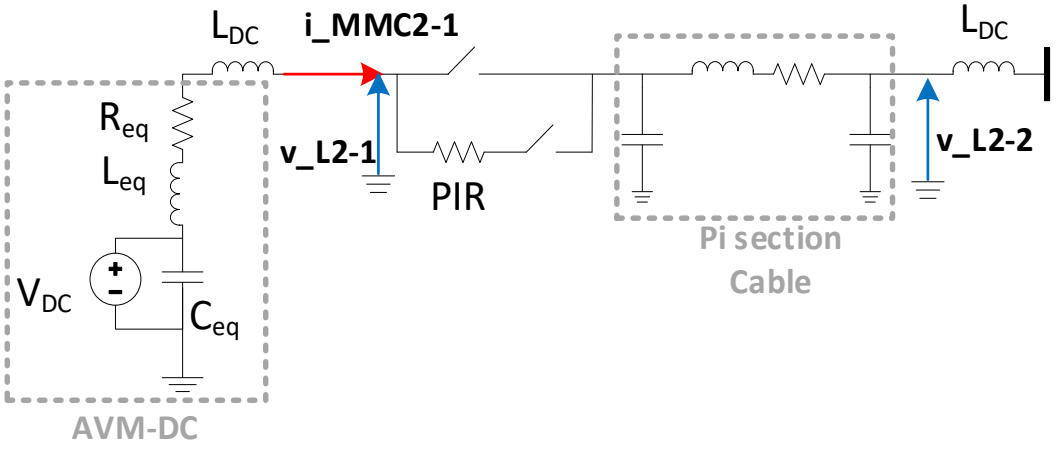


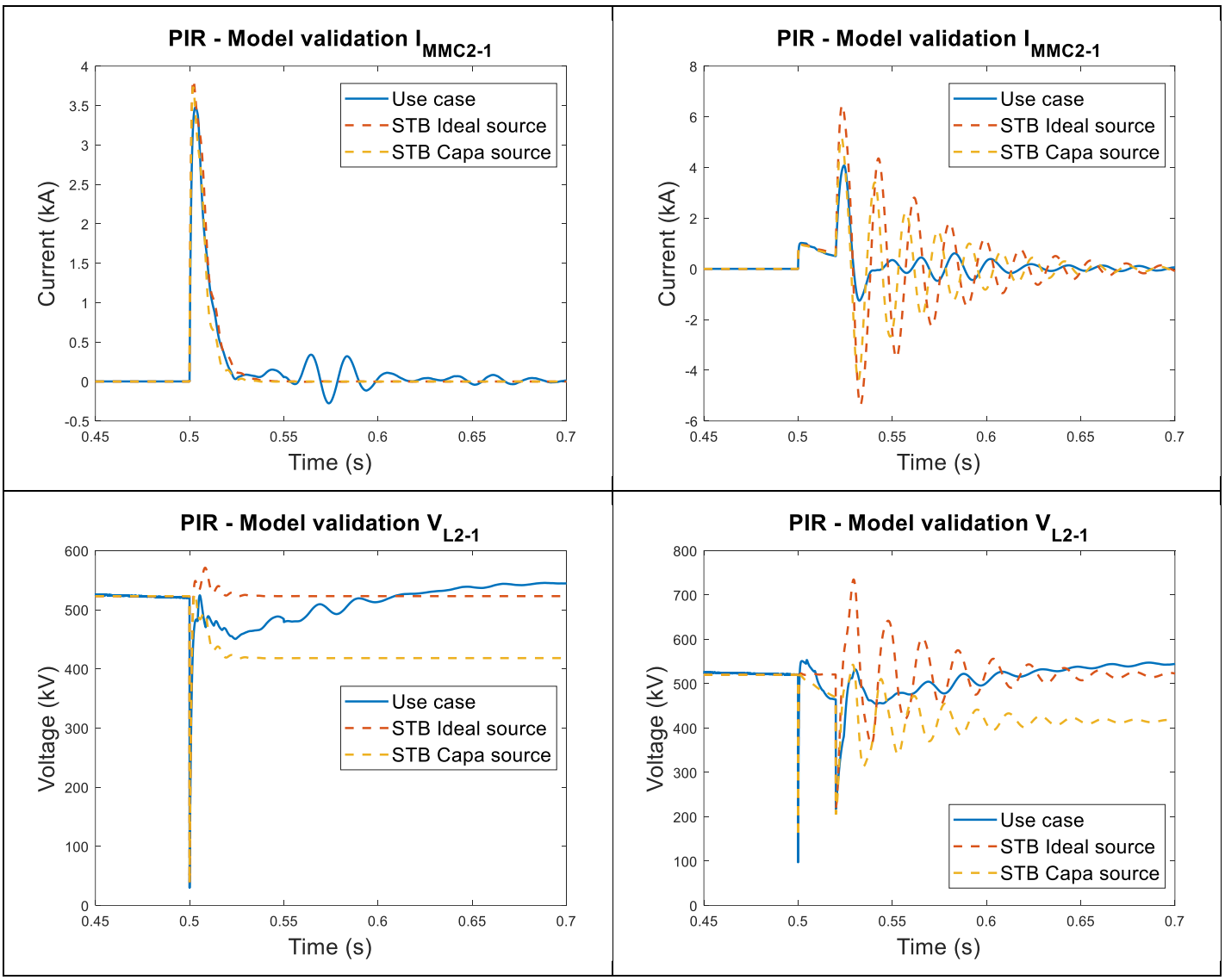
Figure 135: STB for PIR sizing. The voltage source can be disconnected to account for the capacitive discharge only. Current is measured at the closing side while voltage is measured at the open side of the energized cable.

The results of the two variants are compared with the full PSCAD model (connection of line L2 of 400 km from MMC2-1 from use case 1.1) in Figure 136 for the current (left) and the voltage (right). Two different sets of parameters are used: 1) PIR = 100 Ω, EIT = 0.05s, and Ldc = 0.1H (top) ; 2) PIR = 500 Ω, EIT = 0.02 s and Ldc = 0.1H (bottom).

Overall, the STB presents a good fit with the use case at the beginning of the energization (typically during 50ms) but not for longer times. However, the critical behavior (overcurrent, under and overvoltage) occurs at the very beginning. For the first case, the STB shows a particularly good match with use case in terms of peak current and undervoltage. The overvoltage is slightly more difficult to represent, though the capacitive source model gives an accurate overvoltage level. In the second case, the dynamic during the PIR insertion is well represented but is not dimensioning, except for the undervoltage. The overcurrent and overvoltage that occur at the bypassing of the PIR are overestimated, and the capacitive model presents slightly better results. The oscillations that are present in this second case are typically damped by the voltage control, which is not represented in the STB.

Those two sets allow to represent the two main behavior:

- → In the first case (left plots), the cable charging occurs mainly during the insertion of the PIR
- → In the second case (right plots), the dynamic is slowed down due to the large PIR value and the reduced insertion time makes the energization slower. In this case, the bypassing of the PIR (at t =0.52s) creates large current and voltage oscillations. The peak current occurs at this moment. This situation also occurs with large inductance.



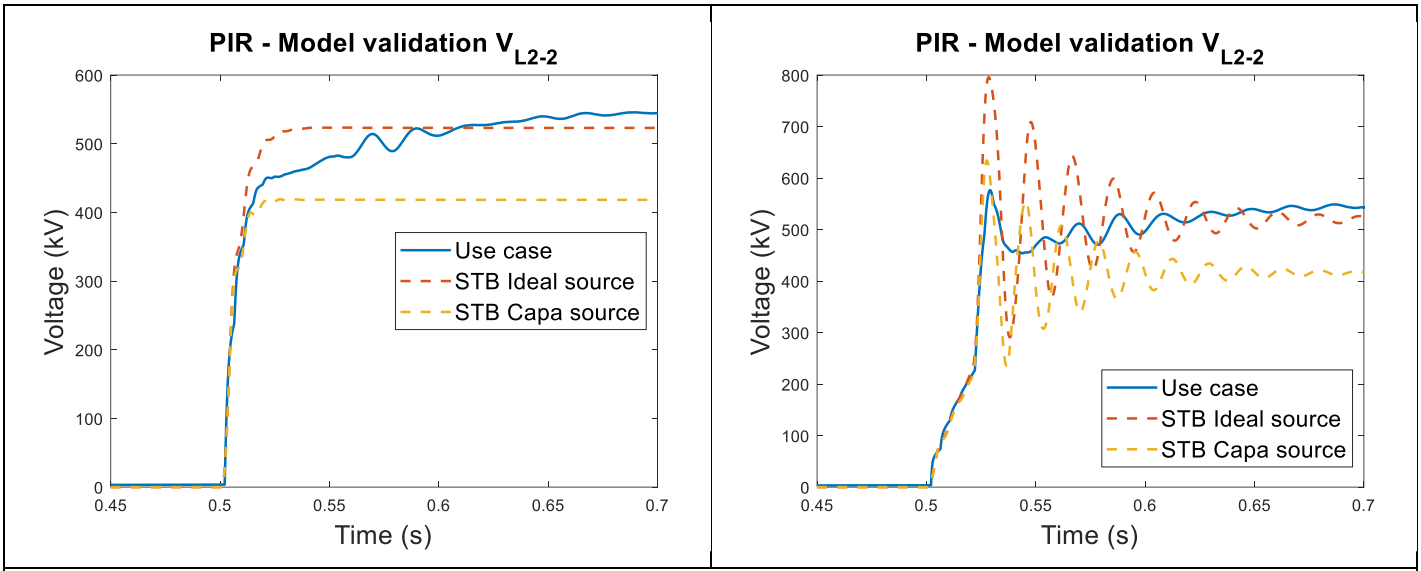


Figure 136: Transient voltage and current during cable energization from a single converter station; Comparison between the proposed STB and the Use case (left: Ldc = 0.1H, PIR = 100Ω, and EIT = 0.05s; right: Ldc = 0.1H, PIR = 500Ω, and EIT = 0.02s)

Based on this section, the STB for cable energization representing the capacitive discharge of the MMC only is selected to study the overvoltage, undervoltage, and overcurrent during the cable energization.

8.2.3. Results for dimensioning test scenario

Extensive simulations were performed to study the impact of the inductor (the same value is used for both line ends), the PIR, and the insertion time on the overcurrent, over and undervoltage, and energy absorption. The AVM-DC model with only the capacitor as a source is used for the extensive simulations as it presents slightly better results, as seen in the previous section. As the three parameters are varied (Ldc, PIR, EIT), the results are presented as contour plots where one of the three parameters is fixed. A cable length of 400km is considered here. The influence of cable length is addressed in Section 8.2.3.4.

8.2.3.1. Overcurrent

The main simulation results for the overcurrent level are displayed in Figure 137, depending on EIT and Ldc for a fixed PIR (left), depending on Ldc and PIR with a fixed EIT (center) and depending on PIR and EIT with a fixed Ldc (right).

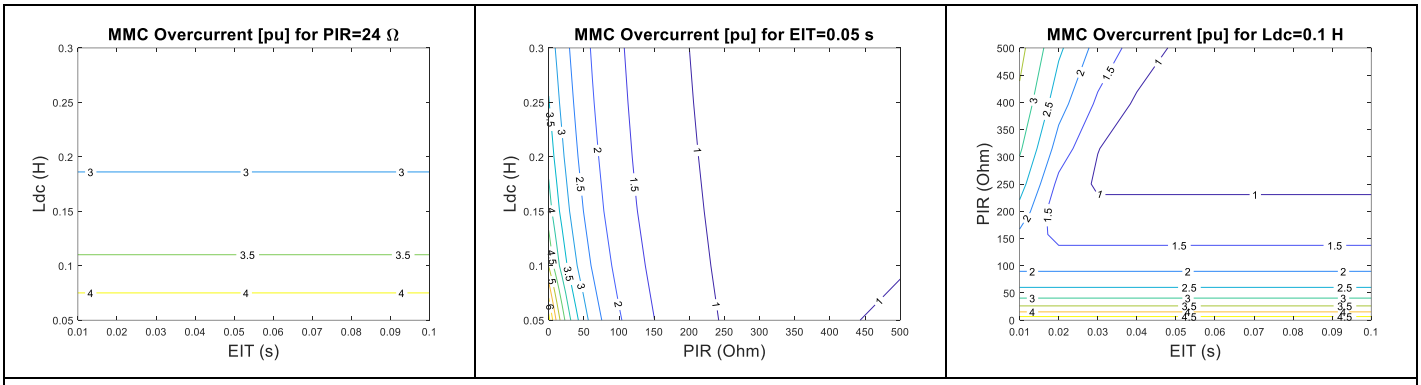


Figure 137: MMC overcurrent levels depending on the PIR size, insertion time and inductance value

Based on the above figure, one can see that

- → Without any DCR, the overcurrent can reach up to 4-5 pu (see center figure). A PIR of about 50 Ohms effectively limits the overcurrent to 3pu.
- → The influence of the EIT is limited to the cases where the energization is slow, due to a large DCR and large PIR (e.g., > 300 Ohms, see right figure). In this case, the PIR should be inserted for a sufficiently long time (e.g., at least 0.03 s).

8.2.3.2. Energy absorption

The amount of absorbed energy by the PIR is presented in Figure 138 in the same fashion as the overcurrent.

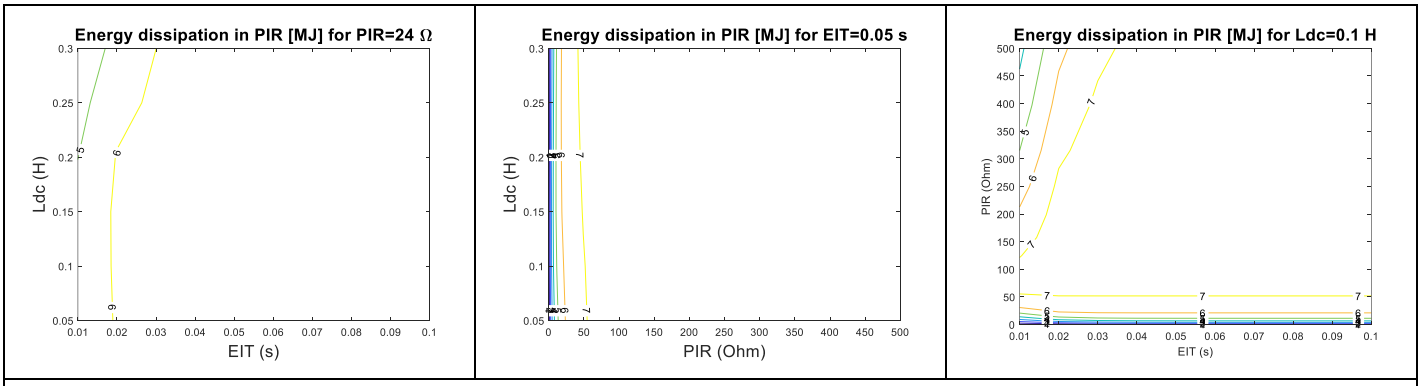


Figure 138: Energy absorbed by the PIR depending on the PIR size, insertion time, and inductance value

The key finding is that the energy absorbed by the PIR does not depend strongly on the DC inductance, the PIR size nor EIT. In particular, it "saturates" at around 7 MJ (for a 400km cable).

8.2.3.3. Over and undervoltage

The overvoltage at the opened end of the cable is presented in Figure 139.

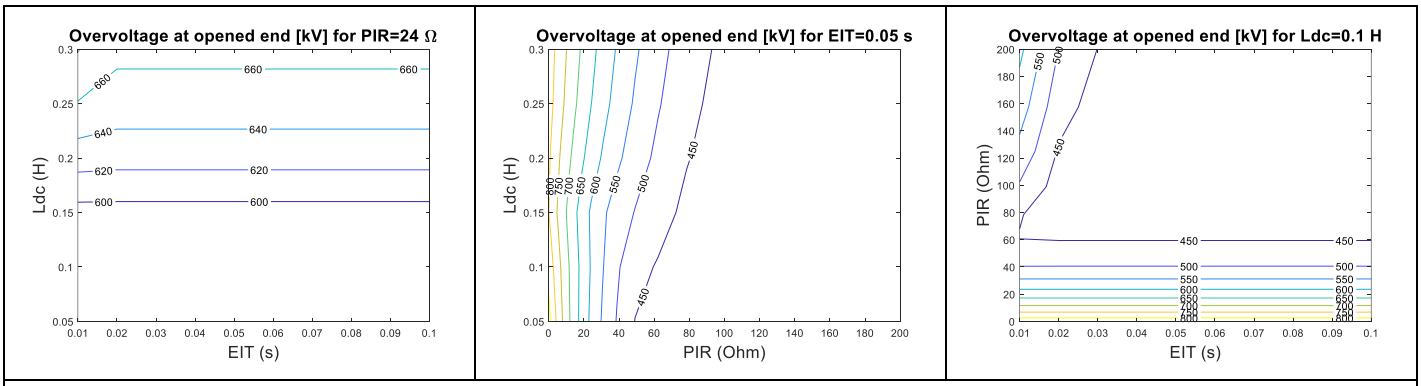


Figure 139: Maximum overvoltage at the opened end of the cable depending on the PIR size, insertion time and inductance value

The overvoltage depends mostly on the PIR size, but overvoltage above 1.7 pu (890 kV) will not be reached. Overvoltage can be limited to a rather small value (<1.2 pu = 630 kV) as soon as the PIR value is above 30-40 Ohms. As for the overcurrent, a higher PIR size combined with a shorter EIT would lead to a higher overvoltage than a smaller PIR with a longer EIT.

Finally, it was observed that the undervoltage does not depend at all on the EIT. Its dependency on Ldc and the PIR is displayed in Figure 140. The undervoltage depends heavily in the inductor size, and typically reaches near 0 V except for large PIR (>200 Ohms). However, this undervoltage typically lasts a few ms which is probably acceptable.

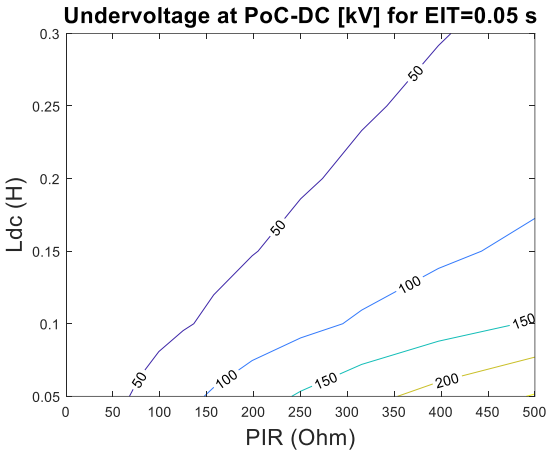
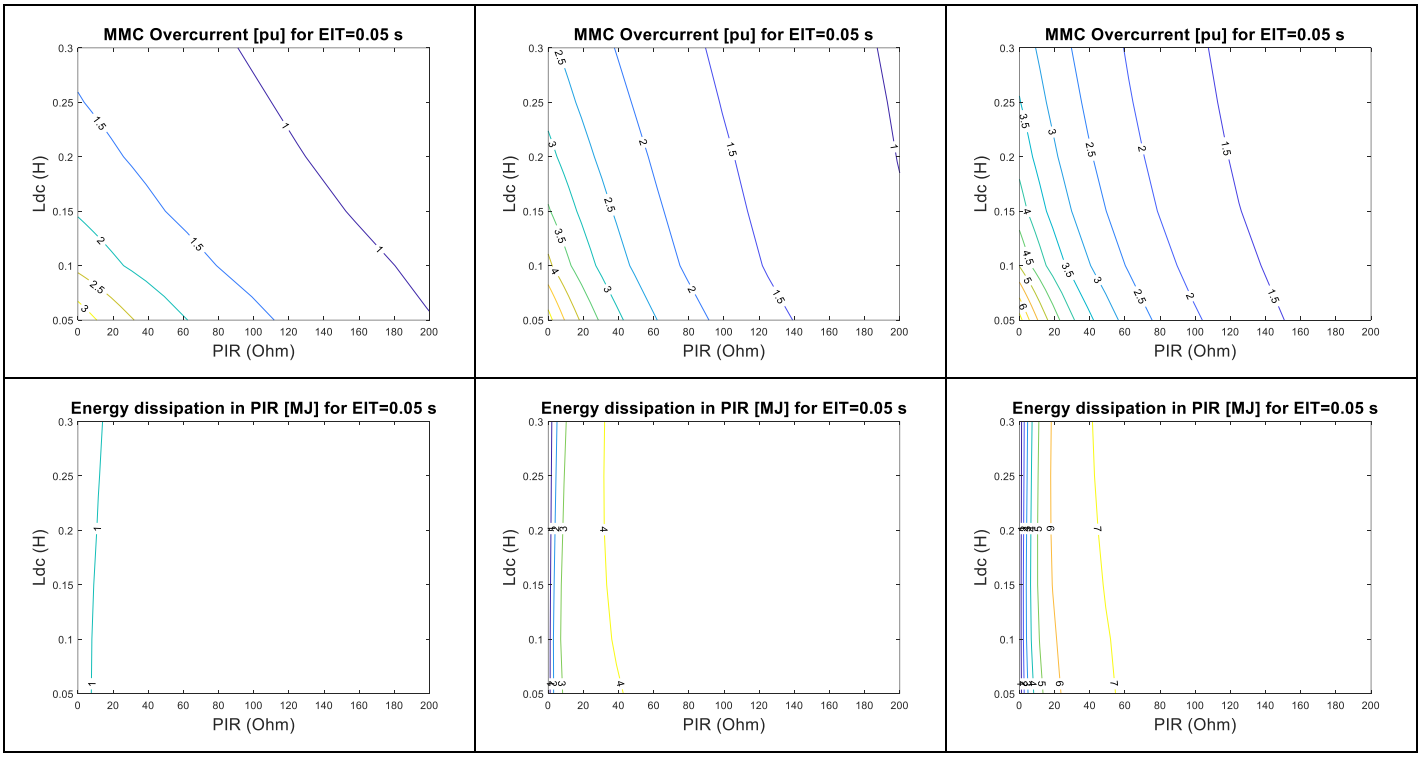


Figure 140: Minimum undervoltage at the PoC-DC depending on the PIR size and inductance value

8.2.3.4. Influence of the cable length

The impact of the cable length on the energization dynamic is now investigated through three representative values: 50km (left), 200km (center), and 400km (right).



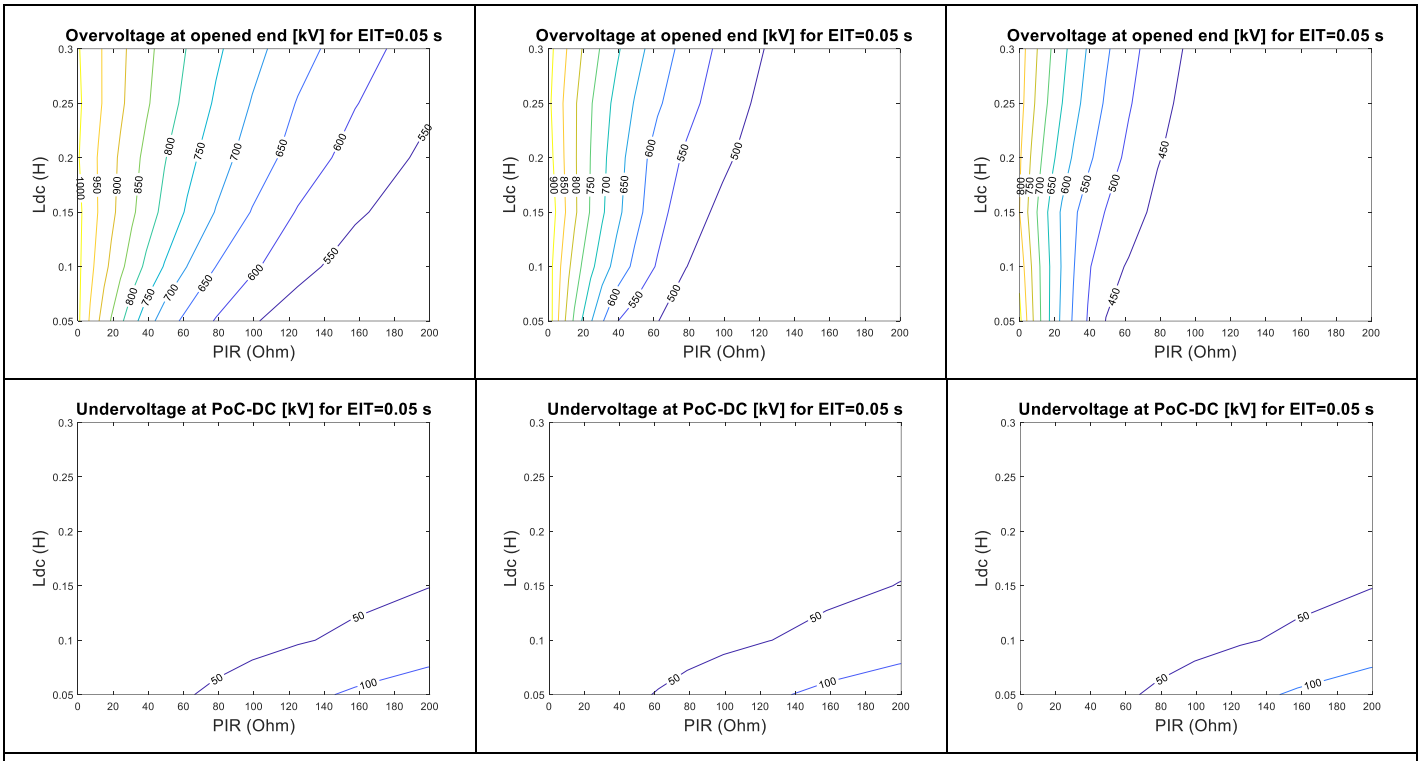


Figure 141: Evolution of overcurrent, absorbed energy, over and under-voltage depending on the PIR size, insertion time and inductance value for three different cable lengths: 50km (left), 200 km (center) and 400 km (right).

The key findings regarding the influence of the cable lengths are

- The undervoltage is not affected by the cable length.
- Overcurrent and overvoltage are influenced in opposite directions. A shorter cable induces lower overcurrent but higher overvoltage. While the overcurrent requirement is dimensioning for long cables, it is the overvoltage for shorter cables (e.g., 50km).
- The energy absorbed by the PIR depends mostly on the cable length and the PIR size, as shown Figure 142.

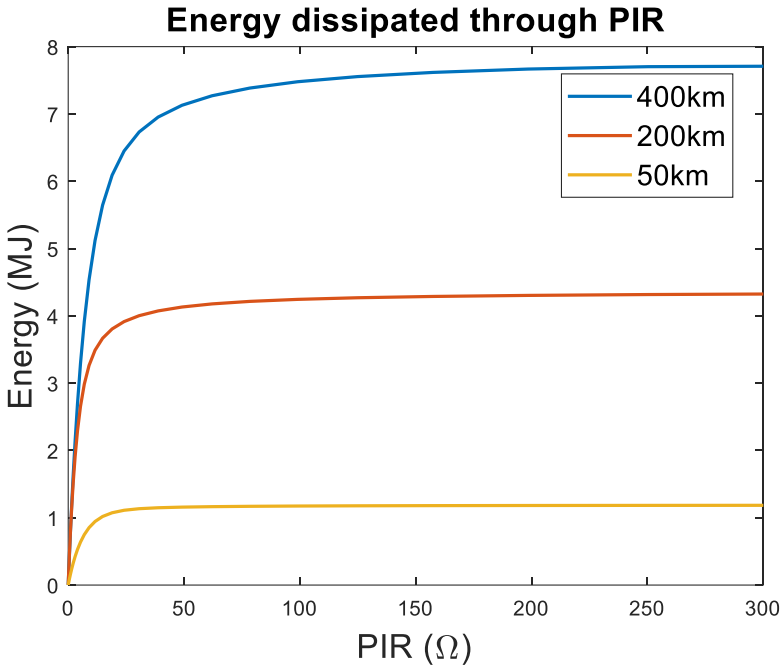


Figure 142: Energy dissipated through PIR as a function of the PIR size, for 400,200, and 50km cables. The DCR is fixed at 300 mH, though its impact is negligible

8.2.4. Conclusion

The parameter ranges determined for cable energization relate to the functional requirement General66.

First, the considered constraints are summarized in Table 63.

Table 63: System constraints to be respected during cable energization

	Value / range	Comment
Max DC overcurrent	4-5 pu	Based on current measured at the DC side, as proposed in section 6.2.1
Max overvoltage	1.5-1.7 pu (800-1000 kV)	Max overvoltage for a duration of 10's ms.

Based on those constraints, the PIR can be designed with the analysis conducted in Section 7.4.3. t was considered that, assuming that the overcurrent and overvoltage requirements are satisfied, smaller PIR are beneficial. Small PIR indeed makes the behavior independent of the EIT, which releases any constraint on this parameter. By contrast, large PIR with small EIT may cause unexpectedly large currents, as seen in Figure 137. In addition, small PIR makes the general response time of the cable energization faster, which is considered beneficial.

Relevant range of PIR design parameters are given in Table 64.

Table 64: Main parameter range for PIR sizing

Design parameter	Parameter range	Comment
PIR size	50-100 Ω	A lower value corresponds to a longer cable, and a higher value to a shorter cable
Electrical Insertion Time	10-50 ms	Assuming PIR and Ldc values in the indicated ranges, the insertion time can be chosen without further impact in this range
PIR energy absorption	1-7 MJ	Depends mostly on the cable length

The determined characteristics address only the energization of cables. A different analysis should be performed to assess the requirements of PIR placed at the DC side of MMC stations to limit overvoltage and overcurrent during uncontrolled charging of a converter. This is addressed in the next section.

8.3. Energization of blocked converter station from DC side

8.3.1. Methodology

Offshore and potentially onshore converter stations are to be energized from DC side during start-up. More generally, a converter that was disconnected, e.g. for maintenance reason, can be energized from the DC side. The uncontrolled charging process consists of the energization of the submodule capacitors, which can induce voltage oscillations and a current surge. Those perturbations should be limited to an acceptable level for the other converters connected to the grid. This can be done by using pre-insertion resistor placed at the output of the converter being connected.

If the DC voltage is not controlled and all other converters are blocked, as for instance during a start-up sequence, constraints on the acceptable overcurrent, overvoltage, etc. are typically not as stringent as for a controlled converter. The connection of a converter to an operational grid should, for instance, not cause the blocking of any other converter due to overcurrent or undervoltage criteria. Thus, it is more relevant to focus on the energization of a blocked converter from a controlled DC grid. For the same reason, the voltage is measured at the output of the controlled converter, rather than at the output of the energized converter which is blocked.

8.3.2. STB: simplified MMC energization from controlled DC grid

The proposed simplistic test benchmark comprises an AVM-DC model using a simplified DC voltage control, and the MMC to be energized is represented as RLC equivalent, as presented in Section 3.5. Cables are accounted for using pi-sections. More or fewer controlled converters and cables can be included in the STB to correspond to a particular scenario (e.g., one or multiple DC voltage-controlled converters).

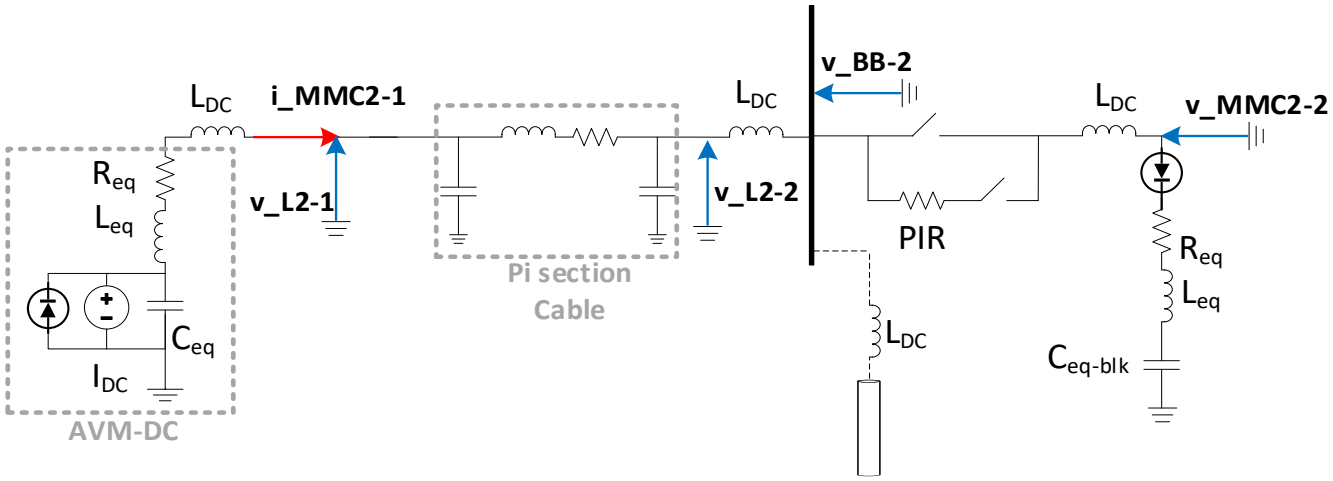


Figure 143: Simplistic Test Benchmark for sizing of MMC PIR

The STB is validated using UC1.1 where the MMC1-2 and MMC2-2 are energized at t=0.6s and t = 1s, respectively. The current and voltage at MMC2-1 are compared for the STB and UC1.1 in Figure 144. The first swings are well represented by the STB, though the following oscillatory behavior is generally less accurate. Overall, the overcurrent, overvoltage, and undervoltage obtained are deemed precise enough to proceed with the STB.

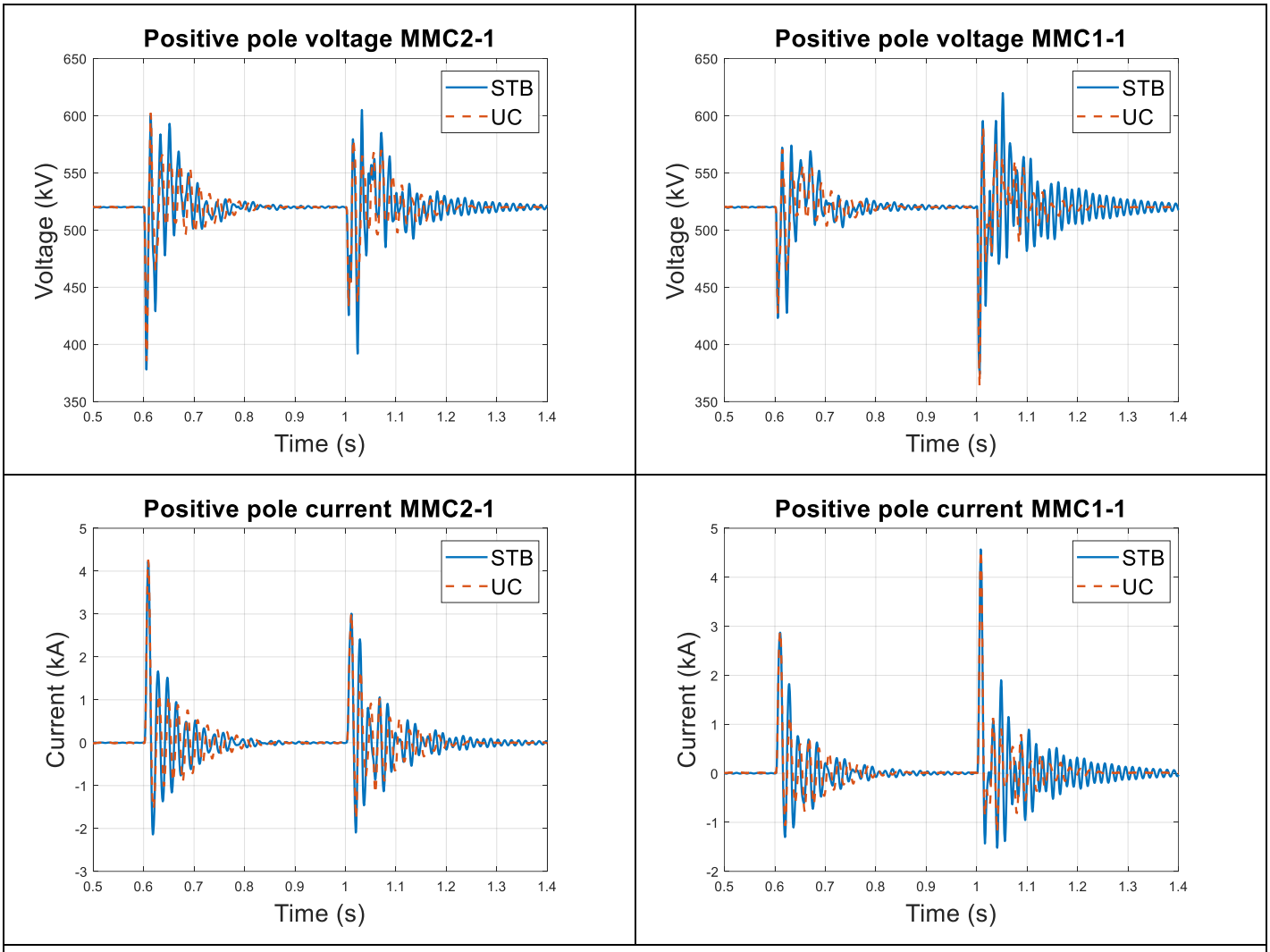


Figure 144: Comparison between STB and UC1.1 for the energization of MMC2-2 and MMC1-2 at t=0.6s & t=1s, respectively. Offshore MMC PIR is 40 Ohms, and DCR = 0.1 H.

8.3.3. Results for dimensioning test scenario

The energization of a converter from the DC side can be performed in various configurations (number of connected cables), which depends on the grid topology. The assessment of worst-case configurations allows to focus on a reduced number of scenarios. We thus compare the transient current and voltage of three representative scenarios based on UC1:

- → MMC2-2 is energized, connected to both onshore converters, and MMC1-2 is disconnected.
- → MMC2-1 is energized, connected to both onshore converters and to the MMC2-2.
- → MMC2-2 is energized connected to a single onshore converter in a Point-to-Point configuration.

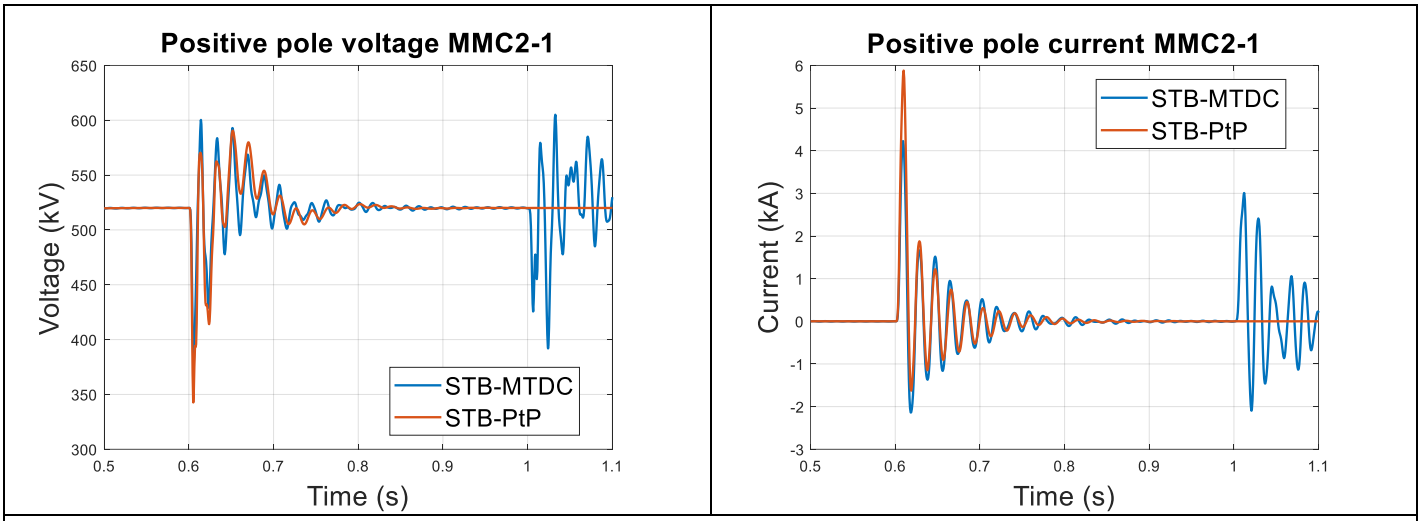


Figure 145: Comparison of different MMC energization scenario using STB. Blue: energization of the first (t = 0.6s) and of the second (t=1s) offshore MMC, connected to two onshore MMC. Red: energization of a single offshore MMC connected to one onshore MMC.

Based on the voltage and current observed at the onshore converters provided in Figure 145, the dimensioning scenarios are

- → For the overcurrent and undervoltage criteria, energization in a PtP configuration
- → For the overvoltage criteria, energization of an offshore converter connected to multiple cables. However, the overvoltage observed in the PtP configuration is rather close to this case.

Overall, the observed overvoltage is modest (<1.2 pu) whereas the overcurrent in the PtP configuration reaches 3pu. It is thus decided to use the PtP configuration as the worst-case scenario for the sizing of the PIR.

The influence of the cable length is investigated in Figure 145 by varying the length from 100 to 400km. The highest overcurrent is reached for a length of 200km, and the lowest undervoltage for a length of 100km. The variation of the overcurrent/undervoltage with the cable length is overall limited. As the overcurrent criteria can be foreseen to be the most critical one, and to limit the number of cases to be examined, a cable length of 200km is considered.

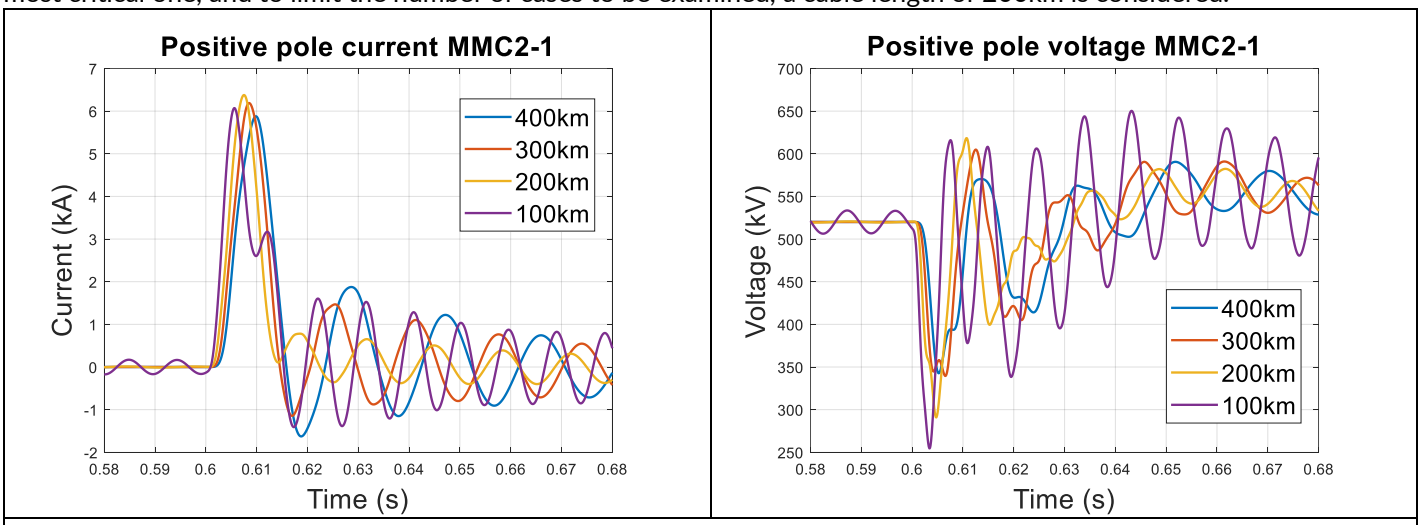


Figure 146: Evolution of the voltage and current during offshore MMC energization in PtP configuration for different cable lengths

Extensive simulations are performed by varying the size of the DCR, PIR, and capacitor size of the MMC. The overcurrent and undervoltage results are given in Figure 147, depending on the PIR size, the MMC energy level, and on the DC reactor. Key observations are:

- → The overcurrent condition appears more dimensioning than the undervoltage, which is generally limited above 0.7pu, except for large submodule capacitors.
- → The overcurrent depends mostly on the PIR and the DCR sizes, and is not much affected by the capacitor size.
- → A PIR of above 50 Ohms allow to limit the overcurrent to 2-3 pu, depending on the capacitor and DCR size.

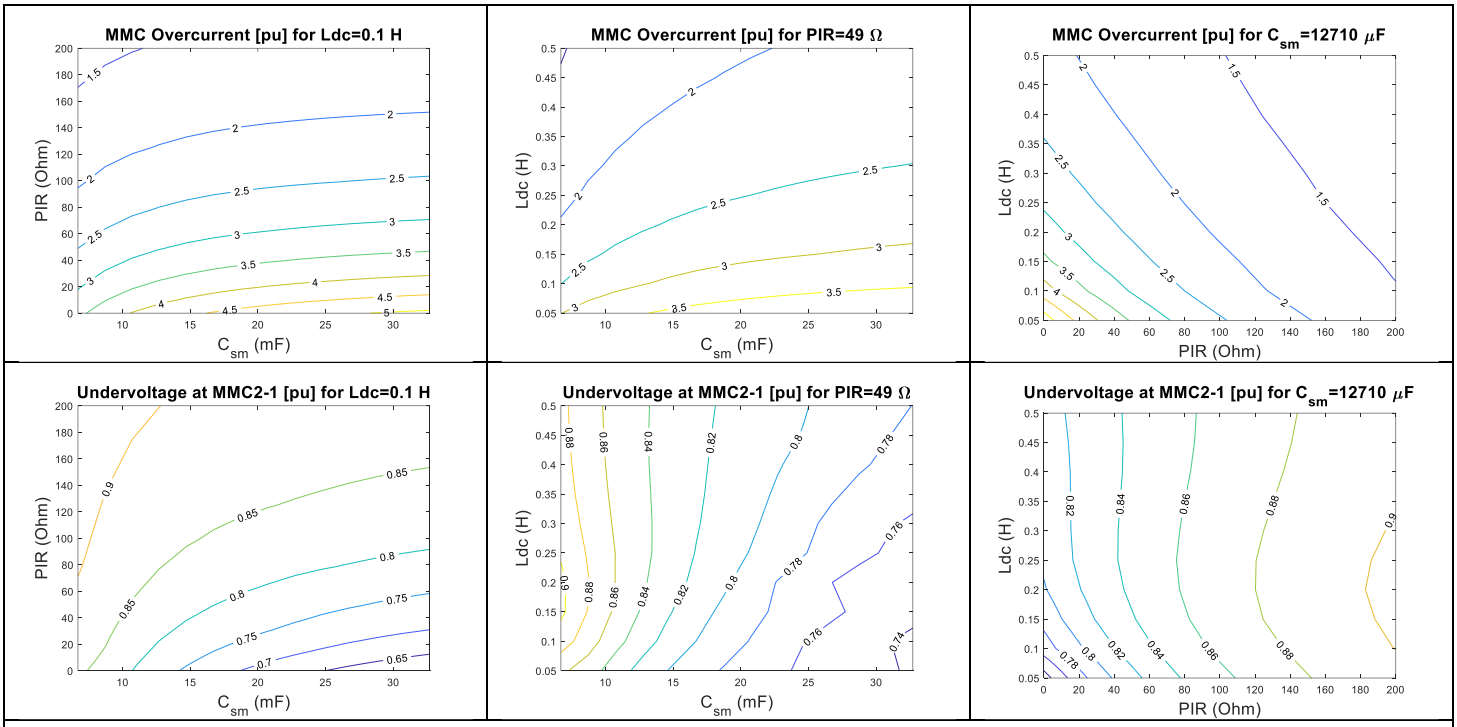


Figure 147: Overcurrent (top) and undervoltage (bottom) in pu during the energization of a blocked converter from the DC side in a PtP configuration depending on the PIR size, MMC submodule capacitor, and DCR size .

Finally, the overvoltage at the output of the onshore converter is evaluated using the same methodology, see Figure 148. The resulting overvoltage is always below 1.2 pu, and is thus non dimensioning, compared to the overcurrent criteria considered above.

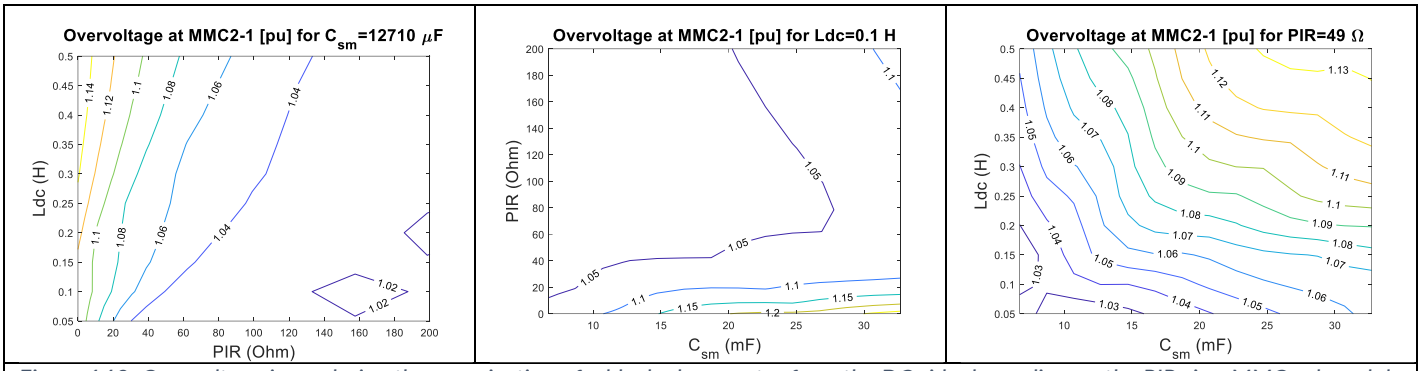


Figure 148: Overvoltage in pu during the energization of a blocked converter from the DC side depending on the PIR size, MMC submodule capacitor, and DCR size

8.3.4. Conclusion

In this section, the transient behaviour caused by the connection and energization of a blocked MMC converter to a controlled DC grid network was investigated. The main dimensioning criteria is the overcurrent at the onshore converter. The influence of different DCR values as well as capacitor size was also studied. Overall, a PIR of above 50 Ohms allow to limit the overcurrent to 2-3 pu, depending on the capacitor and DCR size.

Note that this requirement applies to both onshore and offshore converters, as onshore converters can also be energized from the DC side. Assuming the switching unit at the output of the converter belongs to the converter station, this requirement applies to the converter station rather than to the switching station, though this is mainly a matter of convention. For converters that are connected to a single HVDC cable (typically onshore converters), two PIR will be placed in series, the cable PIR and the converter PIR. Assuming the larger of the two resistors is selected, only one PIR can be kept.

ID	Functional requirement
General69	The overcurrent induced by the connection and energization of a blocked converter to an operating HVDC grid or sub-grid should be limited to acceptable values. This typically requires the use of a pre-insertion resistor at the DC output of the converter.

9. Functional group – Operational Regimes

9.1. Coordination of DC connection modes

9.1.1. Methodology

According to CENELEC standards, DC Connection Modes (CM) are specified

- → Between a converter station and a PoC-DC, reminded in Table 65;
- → Between a switching station and a cable, reminded in Table 66[15].

A diagram of a generic switching station connecting a converter station and two cables is provided in Figure 149. It is based on the CENELEC standards, extended with naming convention from [14]. A list of acronyms is provided in Table 67. A specific grounding unit is added, comprising a solid grounding option through a small impedance Z, and a non-solid grounding through a surge arrester. The proposed diagram is not intended to represent specifically an offshore nor an offshore switching station, but rather to provide a support for the discussion on connection modes and their coordination. Note also that electrical components such as DC reactors or pre-insertion resistors are not specifically represented. They can be considered as part of specific switchgears such as for instance, DCCB for the DCR and substation disconnecting switch for the PIR.

Table 65: DC connection modes between a converter station (CS) and the PoC-DC

Connection mode	**CU1T1**	**CU1T2**	**CU2T1**	**CU2T2**
CS-mode 1	PoC DC1 P1	PoC DC1 R1	PoC DC1 R2	PoC DC1 P2
CS-mode 2	PoC DC1 P1	PoC DC1 R1		
CS-mode 3			PoC DC1 R2	PoC DC1 P2
CS-mode 4				

[15] For simplicity, the connection modes where one HV pole and DMR are used **in parallel** for the neutral path has been omitted (mode 5 and 6 in CENELEC). The benefit of using such a connection mode over HV return path or DMR return path is unclear.

Table 66: DC connection modes of a switching unit (SU) connected to an HVDC transmission line

Connection mode	BB-P1	BB-N	BB-P2	Comment
SU-1	PoC DC2 P1	PoC DC2 R	PoC DC2 P2	Bipolar
SU-2	PoC DC2 P1		PoC DC2 P2	Rigid bipole
SU-3	PoC DC2 P1	PoC DC2 R		monopole P1 (DMR return)
SU-4		PoC DC2 R	PoC DC2 P2	monopole P2 (DMR return)
SU-7	PoC DC2 P1	PoC DC2 P2		monopole P1 (P2 return)
SU-8		PoC DC2 P1	PoC DC2 P2	monopole P2 (P1 return)
SU-9				Both poles disconnected

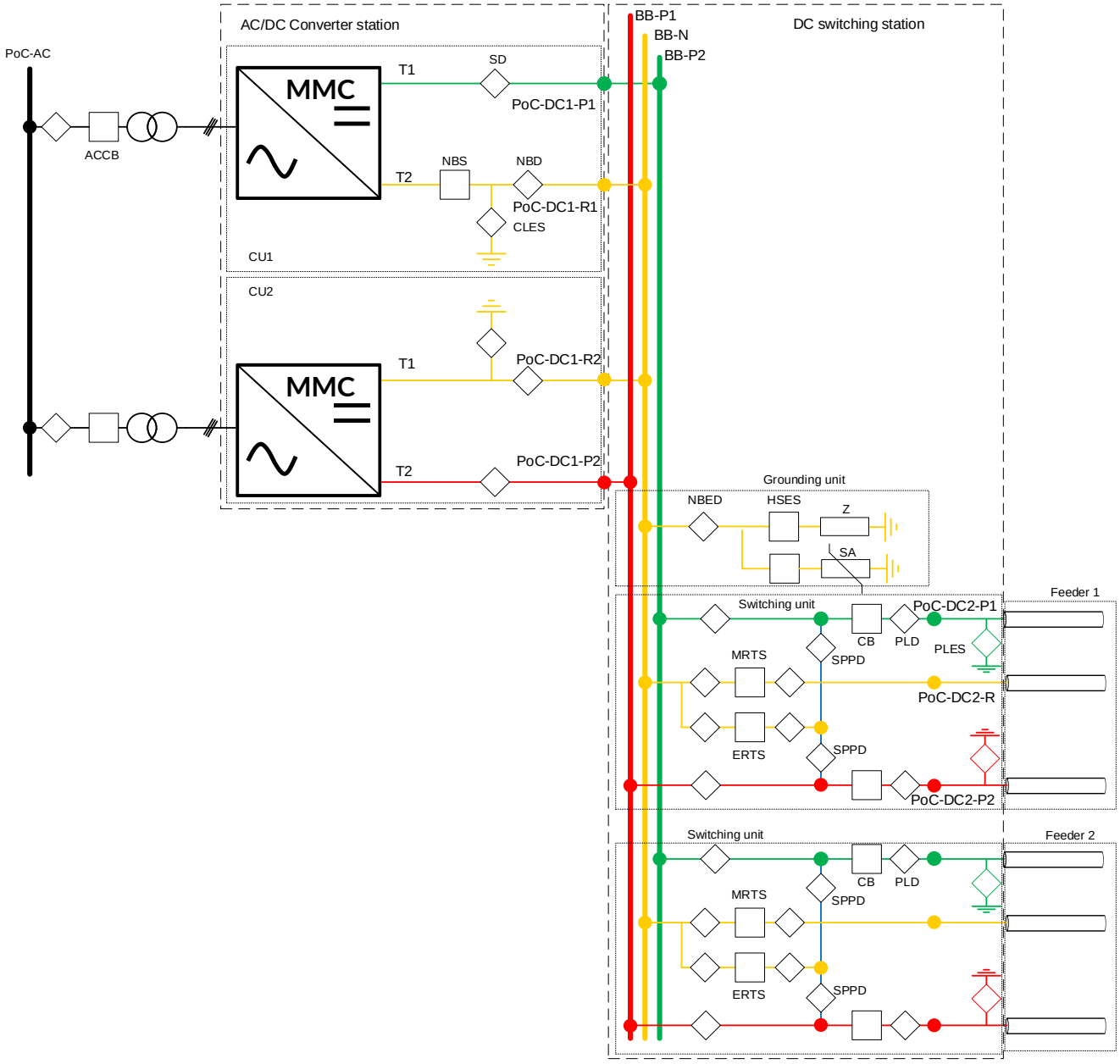


Figure 149: Diagram of a generic switching station connecting a converter station and two feeders

Table 67: Acronyms of the main components considered on the generic switching station

Acronym	Full name
SD	Substation Disconnecting Switch
LD	Line Disconnecting Switch
PLD	Pole Line Disconnecting Switch
NBD	Neutral Bus Disconnecting Switch
NBS	Neutral Bus Switch
NBED	Neutral Bus Earthing Disconnecting Switch
SPPD	Substation Pole Paralleling Disconnecting Switch
PLES	Parallel Line Earthing Switch
PPES	Parallel Pole Earthing Switch
SES	Substation Earthing Switch
HSES	High Speed Earthing Switch
MRTS	Metallic Return Transfer Switch
ERTS	Earth Return Transfer Switch

The coordination of the connection modes (CM) throughout the DC grid consists of

- → Coordination of the grounding. It is considered that the DC grid should always have one solid grounding point. Multiple solid grounding points can be tolerated, temporarily, after a fault or during a reconfiguration. As the DC grid can be operated in degraded modes with unavailable lines/stations, this implies that redundant solid grounding points should be available. In the extreme case where the DC grid is operated as several independent points-to-point links, each onshore station should be solidly grounded. Assuming that an offshore station will always be connected to an onshore station (even if only for startup), the offshore stations do not require a solid grounding option.
- → Coordination of the neutral path. Every converter unit of the HVDC grid that are connected through HV conductors should also share a neutral path. The DC master controller should ensure coordination of the connection modes throughout the grid to ensure this condition is fulfilled in steady-state operation.
- → Coordination of the local connection modes, in particular to ensure the compatibility between the different connection modes.

The compatibility of CM should be ensured at different levels

- → At the DC grid level;
- → Between a converter station and cable connected through the same switching station;
- → Between switching units of the same switching station connecting different cables;

- → Between different switching units connected to the same cable (both ends).

Coordination between different connection modes can then be specified using tables. Two connection modes can be

- → Either impossible due to a voltage difference (e.g., using the same conductor as HV pole and return path)
- → Or possible from the voltage perspective but useless as no current can be transmitted
- → Or suitable

For the coordination of switching unit and converter unit connection modes, two situations should be differentiated:

- → The switching station connects only a converter station with a single transmission line and is composed of a single switching unit. In the context of the use case, this corresponds to the onshore stations.
- → The switching station connects a converter station with more than one transmission line and is composed of several switching units. In the context of the use case, this corresponds to the offshore stations. Offshore stations could also end up in the first situation if, for instance, part of the DC grid is operated as a Point-to-Point.

In the first case, the CM of the switching station is entirely limited by the CM of the converter station. There is for instance no point in connecting both high voltage conductors (SU-1) if one of the converter units is not available (CS-2 & 3) as the power cannot be transmitted.

In the second case on the opposite, the CM of the switching unit(s) can be entirely independent from the connection of the local converter station. If the offshore converter station is, for instance, entirely disconnected (CS-4), the switching units can still be connected in bipolar mode with the rest of the grid. Similarly, both poles of the converter station can still be connected (CS-1) if one of the transmission lines connected to the switching station has an unavailable pole, assuming that another transmission line connected to the same switching station can transmit the power for this pole.

The proposed coordination of the connection modes of a converter station and a switching unit is provided in Table 68.

Table 68: Relevant coordination of connection modes between a switching unit (SU) and a converter station (CS). Green: compatible modes; Orange: Connection modes that should be associated only if an alternative path for the current is available in the rest of the grid.

	CS-1	CS-2	CS-3	CS-4
SU-1				
SU-2				
SU-3				
SU-4				
SU-7				
SU-8				
SU-9				

Compatibility between connection modes of the two switching stations connected to the two ends of the same cable is specified in Table 69 (note the table is symmetric). The limitations are:

- → When used as the neutral path (SU 7 & 8), HV pole cannot be used as HV conductor (SSTL 1 to 4). Such combinations are marked in red.
- → Other configurations where the two switching stations are in different connection modes are feasible but induce a restriction on the power flow. Such configurations may be temporarily relevant (for instance to energize a cable from one end only). Such combinations are marked in orange.

Thus, it seems relevant to ensure that, in **steady-state operation**, **DC connection modes of a cable with the two-switching unit at its ends are identical.**

Table 69: Compatibility and coordination of connection modes of two switching units connected to the same transmission line. Green: Compatible modes; Red: Incompatible modes due to a voltage difference; Orange: modes that are compatible but have a limited power flow.

	SU-1	SU-2	SU-3	SU-4	SU-7	SU-8
SU-1						
SU -2						
SU -3						
SU -4						
SU -7						
SU -8						

Regarding the compatibility of connection modes of different switching units of the same switching stations, no particular constraint arises, and **all connection modes are compatible with one another**.

Finally, the compatibility of the different connection modes at the HVDC grid level is investigated. From the nominal situation where all stations are connected in bipole configuration, several operation modes can be defined:

- One or several onshore stations can be disconnected from the rest of the grid and operate as STATCOM.
- One or several links can be operated as asymmetrical monopole. If a link with an onshore station is operated as an asymmetrical monopole, the converter unit of the unused pole, if available, can be used as STATCOM.
- The disconnection of one interconnector may lead to the division of the HVDC grid into smaller grids. A particular example is the operation of one onshore and one offshore station as PtP.
- The operation of one of the links in rigid bipole, in case of the unavailability of the DMR, raises several issues.
  - In rigid bipolar operation, high probability faults (i.e., internal converter fault) lead to a loss of 2GW compared to 1GW loss in normal bipolar operation.
  - It is assumed that in normal operation, the AC side of wind farm converter poles are decoupled in order to reduce the risk of losing 2 GW in case of an offshore AC fault. Therefore, after a DMR fault, the operation of the grid in rigid bipole with AC coupling of both converters is not considered. This makes the balancing between the two poles more complex.
  - In particular, the prevention of steady-state ground current requires a perfect balancing between the two poles, which is deemed particularly complex within a multi-terminal HVDC grid

→ For the above reasons, the hybrid operation of a link as a rigid bipole within a bipolar MTDC grid was not considered. In case of DMR unavailability, two different choices are instead available

> Operation of the link in asymmetric monopole, using HV as the neutral path (SSTL 7&8).

> Operation of the link in rigid bipole as a PtP disconnected from the rest of the DC grid. Though this option allows the operation of the considered link at full rated capacity, it requires the disconnection of at least another link.

→ The disconnection of one of the links can be limited to the HV poles or also affect the neutral path. In the latter case, the disconnected part must be grounded separately.

9.1.2. Transition sequence between degraded modes

The transition between the different modes of the HVDC grid relies on the control of the connection modes of the different switching stations within the grid. As specified in CENELEC, the transition between two connection modes is specified under no-load condition. As such, the pre-requisite before any change of connection mode is to de-load the affected conductors. This step may require changing the control modes of the converter stations. Depending on the previous configuration of the DC grid as well as the desired subsequent power flow, it may be necessary or not to change the set-points of the wind farms (see the example in Section 8.1.4). In any case, it appears that the DC grid control should be able to unload any of the transmission lines within the grid.

Assuming that a no-load condition has been reached, the transition sequence must be specified. Note that this does not relate only to the connection modes, but may also to the grounding scheme, the neutral path, and the control modes. Examples are given for the following transition:

- Disconnection of a spoke
- Disconnection of an interconnector, which results in the operation of the DC grid in two independent PtP.
- Disconnection of a single pole and partial operation in asymmetric monopole.
- DMR fault and reconfiguration as an asymmetric monopole using one of the HV poles as the neutral path
- Operation in opened and closed ring operation, using use case 2.

9.1.3. Scenario based on use case 1.1

Except for the last one (closed and opened ring operation), the aforementioned transition sequences will be illustrated using use case 1.1 with the starting power flow specified in Table 70. The topology of use case 1.1 is reminded in Figure 150.

Table 70: Considered initial power flow per pole for use case 1.1

Station	Control mode	Active power per pole (GW)
MMC1-1	Droop	-500
MMC1-2	Fixed AC power	1000
MMC2-1	Droop	-1000
MMC2-2	Fixed AC power	500

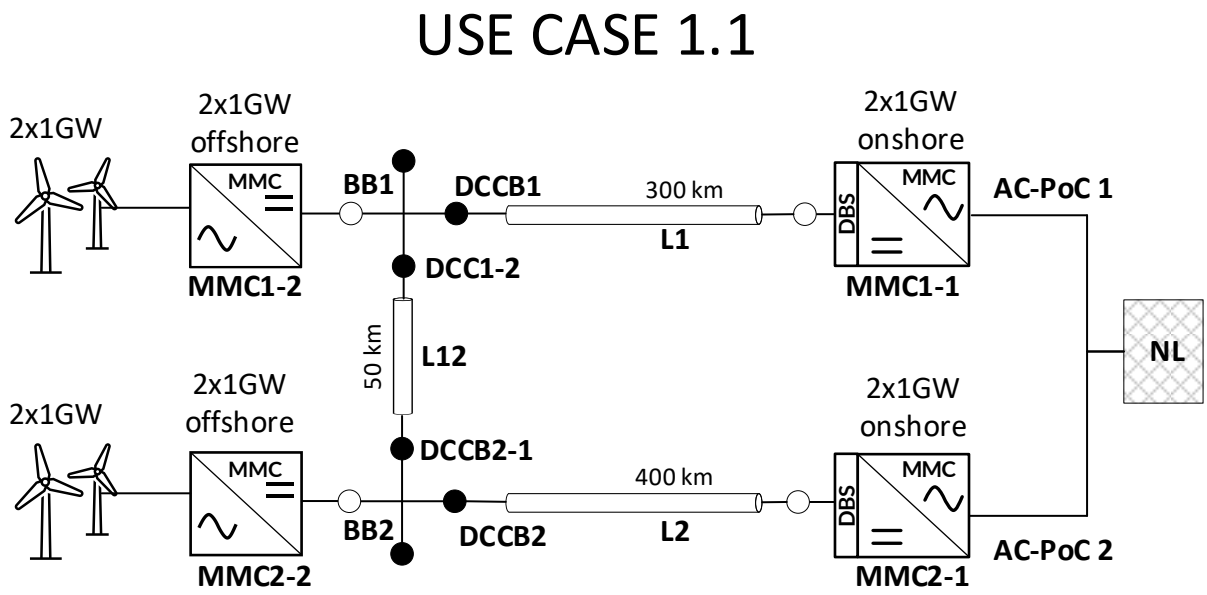


Figure 150: Topology of use case 1.1

9.1.4. Spoke disconnection

The disconnection of a spoke (line 2) in use-case 1.1 is detailed. The following steps are performed, see Table 71. The key aspects are

- → The initial power flow cannot be accommodated without line 1, and one of the wind farms must be partially ramped down.
- → Line 2 is unloaded by setting its active power to 0, which is performed by a change in the applied control mode. Note that the change of control mode in itself is not required and is only used here to ensure the line 2 is unloaded. This could also be achieved using droop control and power flow settings.
- → The use of the line switch to disconnect the onshore side is acceptable as the line has previously been deloaded, and any residual current will be suppressed by the DCCB at the offshore side.
- → The change of the connection mode itself is performed in step 4 and can be considered as nearly instantaneous. The total transition time is mostly determined by the power flow change and ramp down speed.

Table 71: Transition sequence to disconnect line L2

Step	Action	Involved components	Associated time
1	Onshore station 2 is set to power control mode and onshore station 1 to voltage control.	Onshore stations 1 & 2	0.5s
2	Offshore 1 output is reduced to 500 MW (wind farm ramp down)	Wind farm 1	1s
3	New power flow is applied with Pon,2 = 0 MW to unload line 2 (t = 3s)	All converters	3s
4	Line 2 is disconnected using HVDC breaker (offshore side) and line switch (onshore side). DBS at onshore side is also disconnected.	Onshore and offshore switching stations, DBS.	5s
5	Onshore station 2 is set to voltage control.	Onshore station 2	8s

The evolution of voltage, power and current is displayed in Figure 151. The line L2 is effectively unloaded which minimizes the transient at the time of disconnection (t = 5s). The voltage at the disconnected station (MMC 2-1) becomes uncontrollable as soon as it is disconnected from the rest of the grid but is recovered when the station is switched to Vdc control.

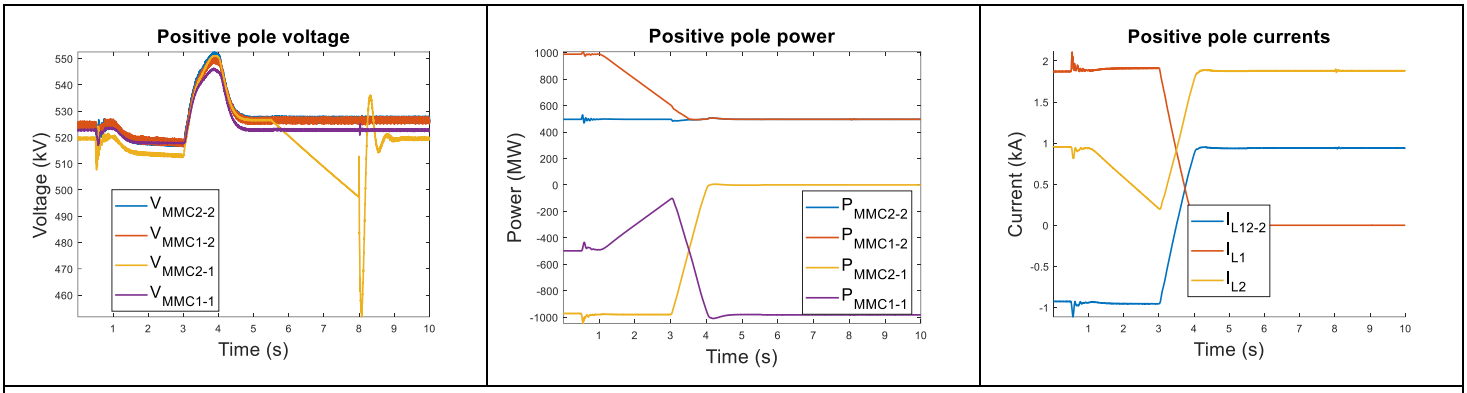


Figure 151: Positive pole voltage, power, and current for the disconnection of line L2 in use case 1.1

9.1.5. From MTDC to PtP operation

The disconnection of the interconnector (line 12) in use-case 1.1 is detailed, which leads to the operation of the grid as two separated PtP. The following steps are performed, see Table 72. The new power flow does not require a reduction in the power output of the wind farm. Step 2 is thus removed. As for the previous case, the change of control mode in itself is not required and is only used here to ensure the line 12 is unloaded. This could also be achieved using droop control and power flow settings.

Table 72: Transition sequence to disconnect line L12 and go from meshed to PtP operations

Step	Action	Involved components	Associated time
1	Onshore station 1 is set to power control mode and onshore station 2 to voltage control.	Onshore stations 1 & 2	0.5s
2	New power flow is applied with Pon,1 = 485 MW to unload line 12 (t = 3s)		0.5s
3	Line 12 is disconnected using HVDC breakers.	Onshore and offshore switching stations, DBS.	3s
4	Onshore station 1 is set to voltage control.	Onshore station 1	3.1s

In the case where the DMR is also to be disconnected. An intermediate step is performed just before the line disconnection (t = 2.9s). The evolution of voltage, power and current is displayed in Figure 152 for the case where the DMR is also disconnected. The temporary operation of the grid with two solid grounding points does not cause any disturbance.

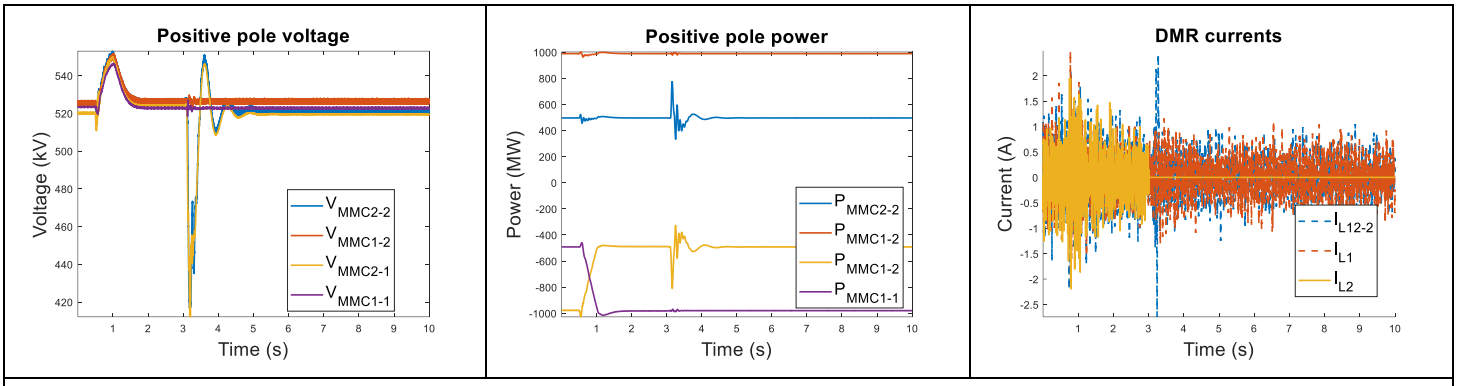


Figure 152: Positive pole voltage and power, and DMR current for the disconnection of line L12 in use case 1.1, including DMR.

9.1.6. Asymmetric monopole

The use of asymmetric monopole configuration is appropriate in several situations:

- → One converter unit is unavailable. In this case, the connection modes of the switching unit with the cable remains unchanged, and only the unavailable converter unit is disconnected.
- → One HV pole is unavailable. In this case, the unavailable conductor is disconnected but both converter units can remain connected if the power can be exchanged on both poles. If the unavailable conductor belongs a spoke connection, there is no alternative to transmit the power of the available pole and the converter unit can operate as STATCOM.
- → The DMR is unavailable. The remaining HV pole can be used as the neutral path, which amounts to the previous case. The HV pole must however first be discharged. Note that the converter unit usually connected to the pole used as DMR can remain connected and operated if an alternative path (other transmission path) is available for this pole at the switching station. If on the contrary the converter is only connected to the affected transmission line, this converter unit cannot transmit power and can only be used as STATCOM.

The first case is illustrated with the disconnection of the negative pole of offshore MMC1-2. The windfarm connected to this converter must first be ramped down to reach 0 power. A new power flow is then applied to take into account the reduced generation. Finally, the converter unit of MMC1-2 connected to the negative pole is disconnected, using first the offshore AC side breaker. Note that in this case, the connection mode of MMC1-2 is CS-2 (according to Table 65) as the second converter unit is disconnected. However, both switching units of the switching station at bus 2 are in the mode SU-1 (bipole) as a current path is available, including for the negative pole.

The proposed transition sequence is presented in Table 73.

Table 73: Transition sequence to disconnect negative pole converter unit of MMC1-2

Step	Action	Involved components	Associated time
1	Onshore station 1 is set to power control mode and onshore station 2 to voltage control.	MMC1-1 and MMC2-1	0.5s
2	Wind farm 2 (negative pole) is ramped down to 0	OWF-1	0.5s
3	New power flow is applied to restore the power reference at MMC1-1	All converters	3.5s
4	AC side breaker of MMC1-2 is open.	OWF 1	5.6s

The evolution of voltage, power and current of the negative pole at the output of the converter stations are displayed in Figure 153 as well as the current in the DMR in all lines. The positive pole quantities are nearly constant during the whole sequence.

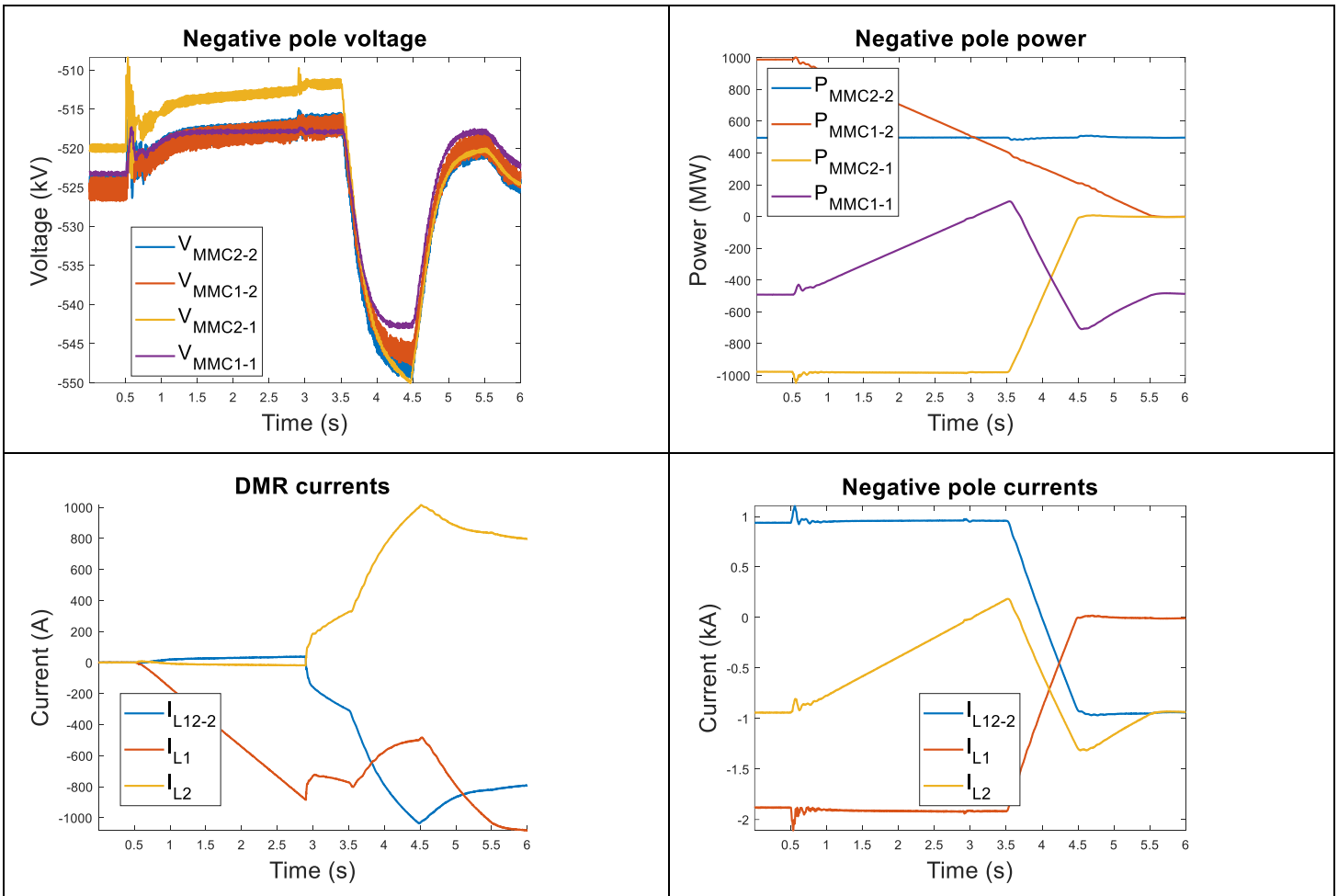


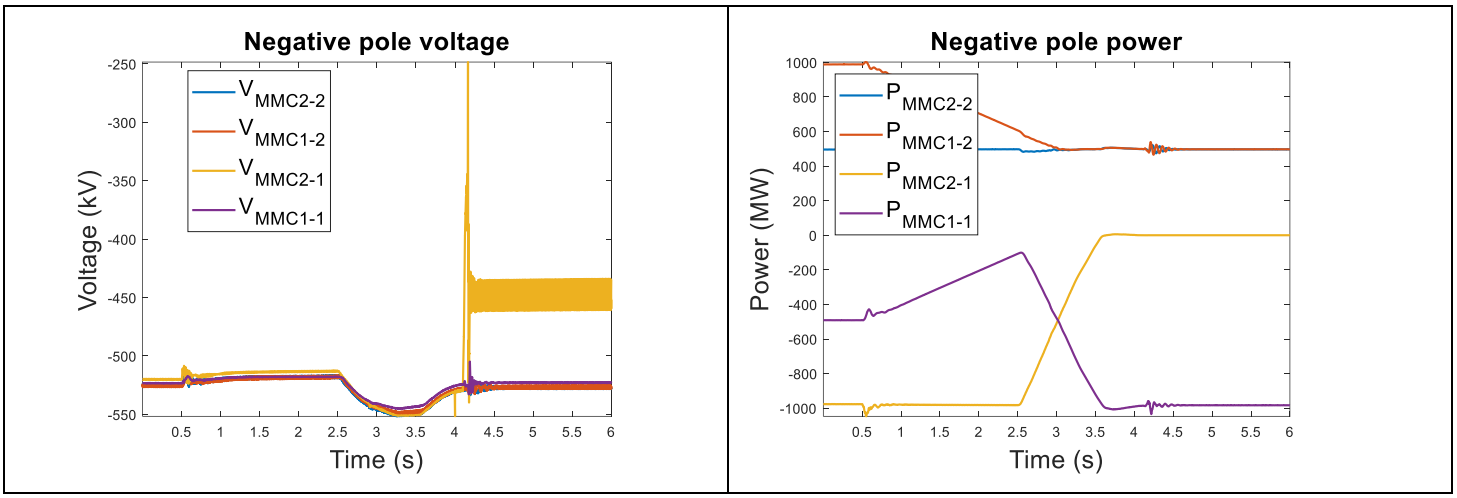
Figure 153: Negative pole voltage and power (top), and current (bottom) for the disconnection of negative pole converter unit of MMC1-2 in use case 1.1

The second case is illustrated with the disconnection of the negative pole of line L2. The power output of wind farm 1 must be reduced to 500MW on the negative pole as the HVDC grid transmission on the negative pole has been reduced to 1GW. The proposed transition sequence is detailed in Table 74.

Table 74: Transition sequence to disconnect negative pole converter unit of line L2

Step	Action	Involved components	Associated time
1	Onshore station 1 is set to power control mode and onshore station 2 to voltage control.	Onshore stations 1 & 2	0.5s
2	Wind farm 1 (negative pole) is ramped down from 1 GW to 500 MW.		0.5s
3	New power flow is applied with Pon,1 = 1 GW for negative pole to unload line 2 negative pole		2.5s
4	Line 2 negative pole is disconnected using HVDC breaker (offshore side) and line switch (onshore side).	Onshore and offshore switching stations, DBS.	4s
5	Onshore station 2 is set to droop control.	Onshore station 1	4,1

The evolution of voltage, power and current of the negative pole at the output of the converter stations are displayed in Figure 154 as well as the current in the DMR in all lines. The positive pole quantities are almost constant during the whole sequence.



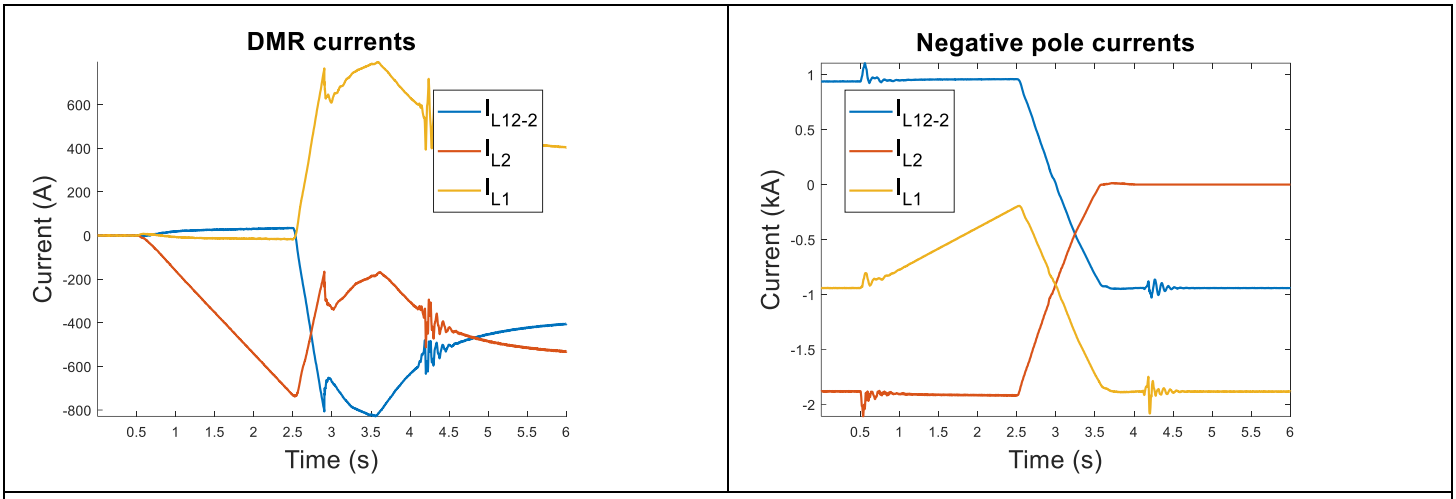


Figure 154: Negative pole voltage and power (top), and DMR and negative pole current (bottom) for the disconnection of negative pole of L2 in use case 1.1

9.1.7. DMR Fault/unavailability and reconfiguration

In this section, the scenario of the unavailability of the DMR is investigated. The following hypotheses were made

- → In case of a DMR fault, it is suitable to rebalance the grid, thus unloading the faulted DMR, before the opening of the DMR. Assuming this, the case of a DMR fault is nearly identical to the case of a planned unavailability of the DMR. Without loss of generality, only the former is thus detailed.
- → A ground current up to the nominal load current can be tolerated for a few seconds. Double grounding of the MTDC system is thus temporarily allowed while floating grid should be avoided.
- → In the reconfiguration process, the operation of the link without DMR as a rigid bipolar connected to the remaining bipolar MTDC is not suitable (see Section 9.1.1 for rationale behind this choice). Alternatively, this link can be operated as an asymmetric monopole, using one of the two HV poles as DMR.

The impact of those assumptions will be highlighted in the following.

Before the fault is applied, an unbalanced power flow was intentionally applied to have a current through the DMR, see Table 75.

Table 75: Initial unbalanced power flow before DMR fault inception

Power generation		**Power absorption**	
Wind farm 1 – positive pole	500 MW	MMC1-1 – positive pole	500 MW
Wind farm 1 – negative pole	1 GW	MMC1-1 – negative pole	500 MW
Wind farm 2 – positive pole	500 MW	MMC2-1 – positive pole	500 MW
Wind farm 2 – negative pole	500 MW	MMC2-1 – negative pole	1 GW

After the fault inception, the complete fault clearing, and reconfiguration is detailed in Figure 114.

Table 76: Fault clearing and reconfiguration sequence in case of DMR fault

Action	**Start time (s)**
MR Fault in L2	0.1
Reduce wind farm 1 negative pole output to 0,5 GW and set Power of MMC2-1 to 0	0.5
Open positive pole breaker of L2	3
Close High Speed Earthing Switch (HSES) at MMC2-1	3
Open Metallic Return Transfer Switch (MRTS) switch of L2	3.1
Discharge the positive pole of L2 (Pole Line Earthing Switch)	3.1-3.3
Connect Positive pole of L2 to neutral bus at MMC2-1 by closing Substation Pole Paralleling Disconnecting Switch (SPPD)	3.4
Open HSES at MMC 2-1	3.5
Ramp up wind farm 1 negative pole back to 1GW and MMC2-1 negative pole to 1 GW	3.5

The power of the four MMC stations during the whole sequence are given in sequence. Figure. The power of the positive pole of MMC2-1 is ramped down before this pole is disconnected and then used as DMR. The balancing of the grid requires the ramping down of the negative pole of wind-farm 1 as the MTDC grid will temporarily be able to transmit only 1GW per pole. This can be seen as a worst-case scenario as, in a larger grid or if less wind power is generated, the balancing of faulted line may only involve the power reference of the converter stations, and not the wind farm generation. Note that the change of power flow for converter station (1pu/s) is faster than the one for the ramping down of the wind farm (0.2 pu/s). At about t = 3s, the grid is balanced as the power on the two poles are identical on each line.

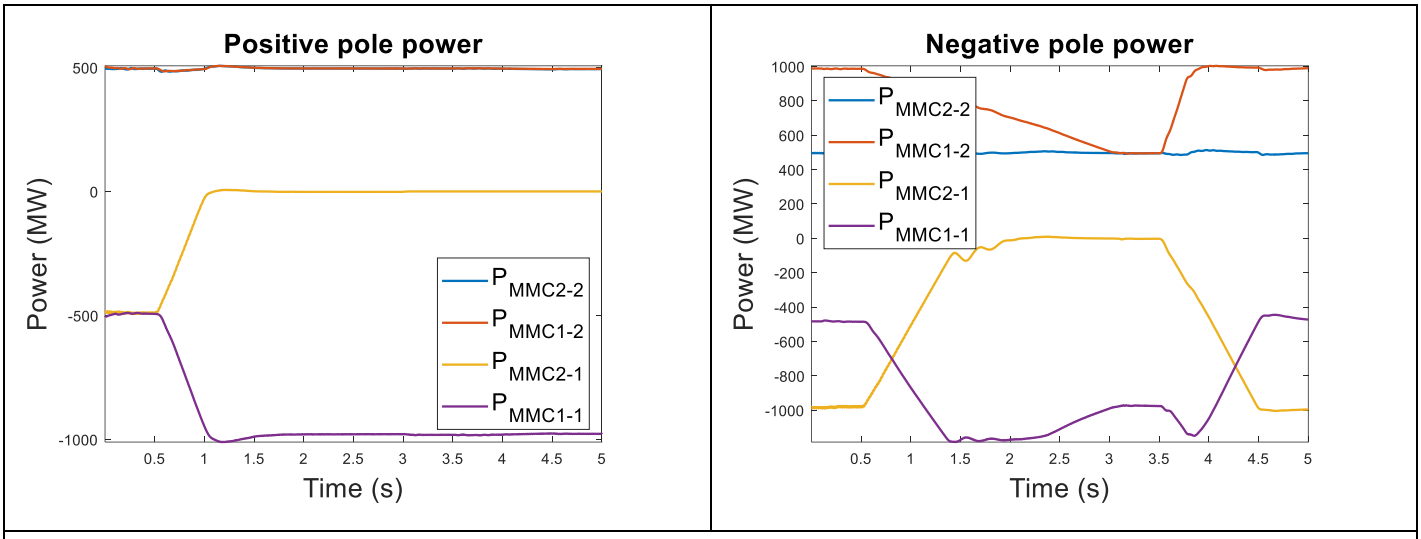


Figure 155: MTDC power for the positive (left) and negative pole (right) during the DMR fault and reconfiguration sequence

The evolution of the currents for the three lines and the three conductors is shown in Figure 156.

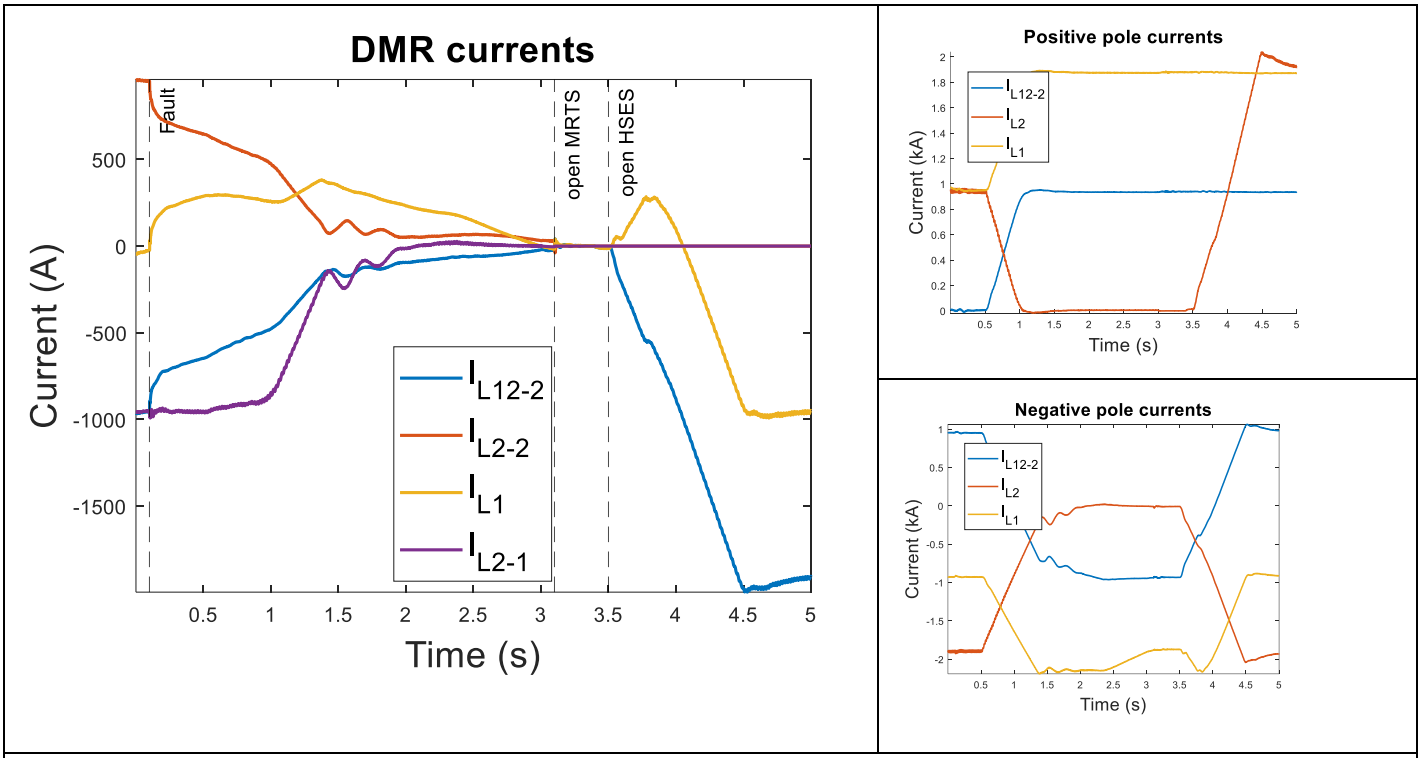


Figure 156: Evolution of the line currents during the DLR fault and reconfiguration for the DMR (left), positive pole (top-right) and negative pole (bottom-right)

A focus on the operation of the neutral bus switchgear at MMC2-1 is provided in Figure 157. The closing of the HSES at t = 3s creates a new path for the current through ground. The residual ground current is commutated to this path at t = 3.1s when the MRTS is opened. As the current is transferred, the resulting voltage across the MRTS is rather small (< 10 kV, see right plot). Between 3.1s and 3.4s, the positive pole, which is disconnected from the rest of the grid, is discharged (see detailed for pole discharge in Section 9.3.2). The connection of the positive pole as DMR at t=3.4s gives again an alternative path for current which makes

it possible to commutate the ground current at t=3.5s by the opening of the HSES. For convenience, the power ramp up in line L2 is started at t=3.5s which explains the fast increase of current through the SPPD.

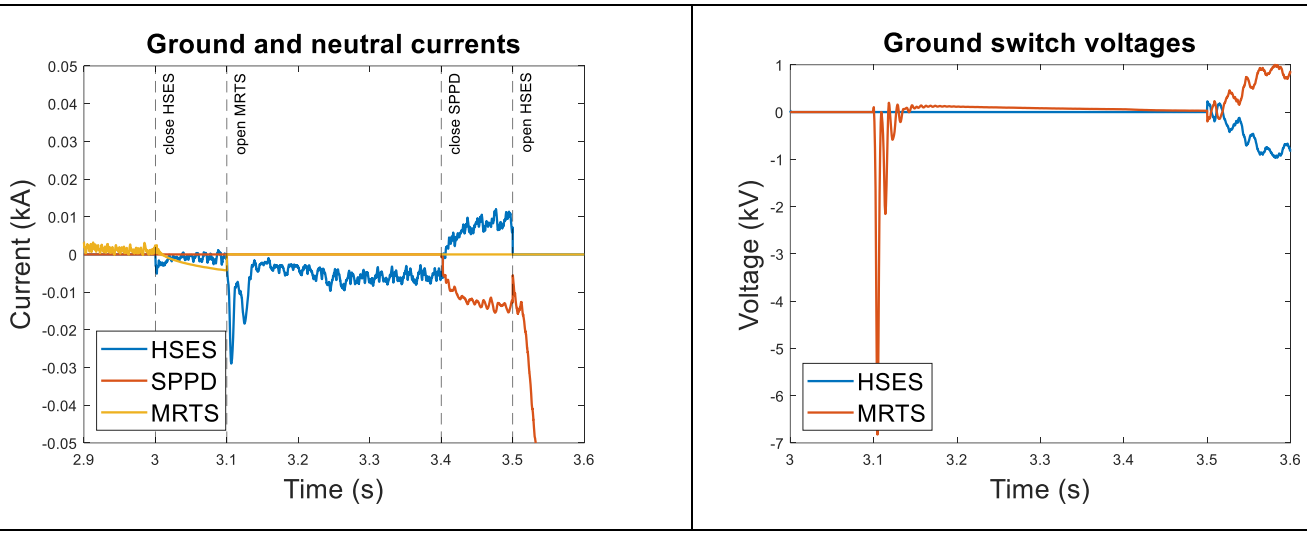


Figure 157: Current (left) and voltage (right) across key switchgear at MMC2-1

Some key observations are

- → The assumption that the grid could be rebalanced prior to the clearing of the DMR fault, as well as the possibility to tolerate double grounding for a short period, makes the switchgear requirements less demanding. The constant availability of an alternative path for ground/neutral currents implies the MRTS and HSES always transfer current but never interrupt it. If the DMR fault has to be cleared prior to the grid rebalancing, the transfer switch capability should be up to the nominal load current.

- → Available ramp up/down speed for power converters and wind farms makes the balancing process possible in a few seconds (3.5s in the example), for which it is assumed the ground current can indeed be tolerated.

9.1.8. Opened and closed ring operation

In this section, the transition between opened and closed ring operation is investigated using use case 2. Starting from an opened ring configuration with the interconnector between spoke 4 and 2 opened, the following sequence is applied. In contrast to the previous cases, the sequence is performed in onload conditions. Indeed, in the meshed topology of use case 2, it may not be possible to control the current flowing through the interconnectors 24 and 13 as the power flow will be established according to the impedance of the different paths. Note that interconnector 24 here refers to the two cables (of length 150 and 300km) that connect the hub 2 and 4.

Action	Time (s)
Connection of L26 and L45 to connect hub 4 to hub 2 and operated in closed ring configuration	3.6
Disconnection of L13 and operation in opened ring	4.5
Reconnection of L13 and operation in closed ring	5.2

The current in the two main interconnections under study (L31 and 42) and the offshore voltages are depicted in Figure 158. The current presents a large spike at the closing of L42 due to the cable energization. This overcurrent is however limited to an acceptable level by a PIR of 50 Ohms. During closed ring operation (between 3.6s and 4.5s, and after 5.2s), the steady-state current through L42 is negligible, compared to the current through L31, as the DC resistance of the path through L42 (450km) is larger than through L13 (200km). The voltage variations are particularly small during the entire sequence.

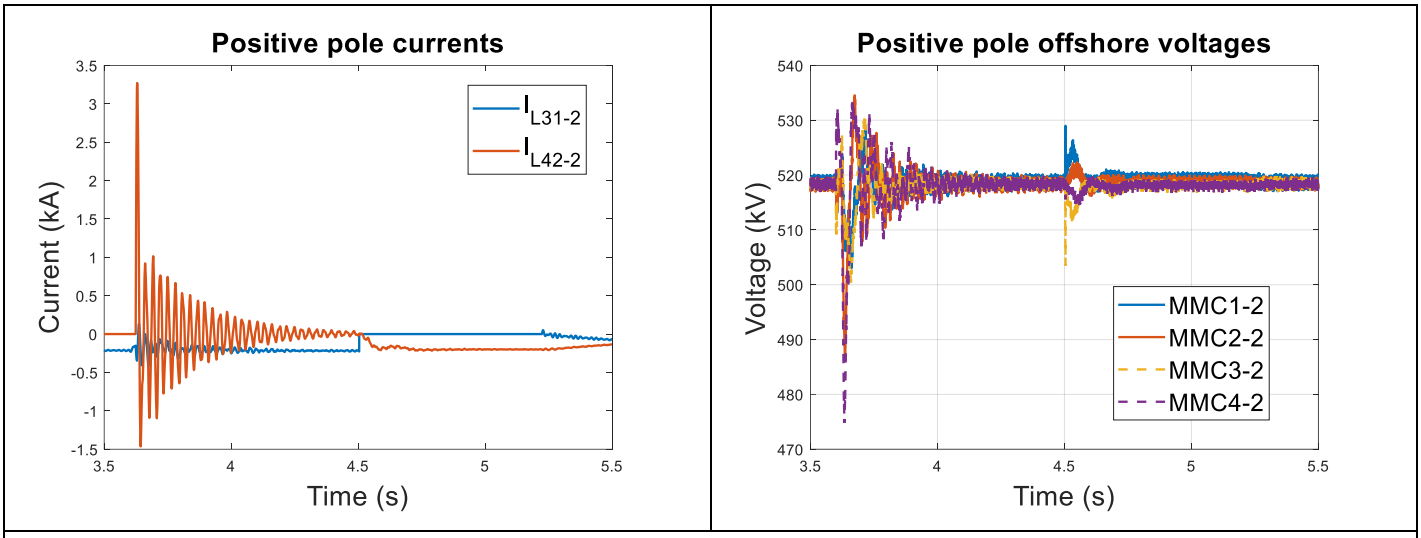


Figure 158: Current in interconnectors L31 and L42 (left) and offshore station voltages (right)

9.1.9. Conclusion

Based on the qualitative analysis and quantitative examples provided in the previous sections, functional requirements are formulated.

ID	Title	Functional requirement
Master_Control6	Operational simplification	The DC grid controller shall be capable of providing operational simplification for the HVDC grid system by default scenarios. This include, but is not limited to, reconfiguration after HV pole unavailability fault, DMR unavailability, converter unit unavailability, at any location within the grid. The considered operational simplification shall ensure the secure operation of the DC grid throughout the process, including the monitoring of the power flow and grounding.
Master_Control10	Coordination of DC connection modes	The DC grid controller shall coordinate the DC connection modes of the switching units and the converter stations throughout the grid. It should ensure the voltage compatibility of the connected conductors and that a current path is always available for on-load operation.
Master_Control11	Coordination of HVDC grid earthing	The DC grid controller shall ensure that the HVDC grid is always solidly grounded in at least one point. Two solid grounding points can be tolerated during a transition sequence.
Master_Control12	Coordination of neutral bus switches	The DC grid controller shall ensure that all HVDC grid installations that share an HV pole are connected to the same neutral point through a dedicated conductor.

9.2. Operating sequences

9.2.1. Methodology

Operating states are specified for single devices, may it be a converter unit, switching unit, or another installation. As the converter units are the **main active components** of the considered HVDC grids, we focus on the operating states of AC/DC converters.

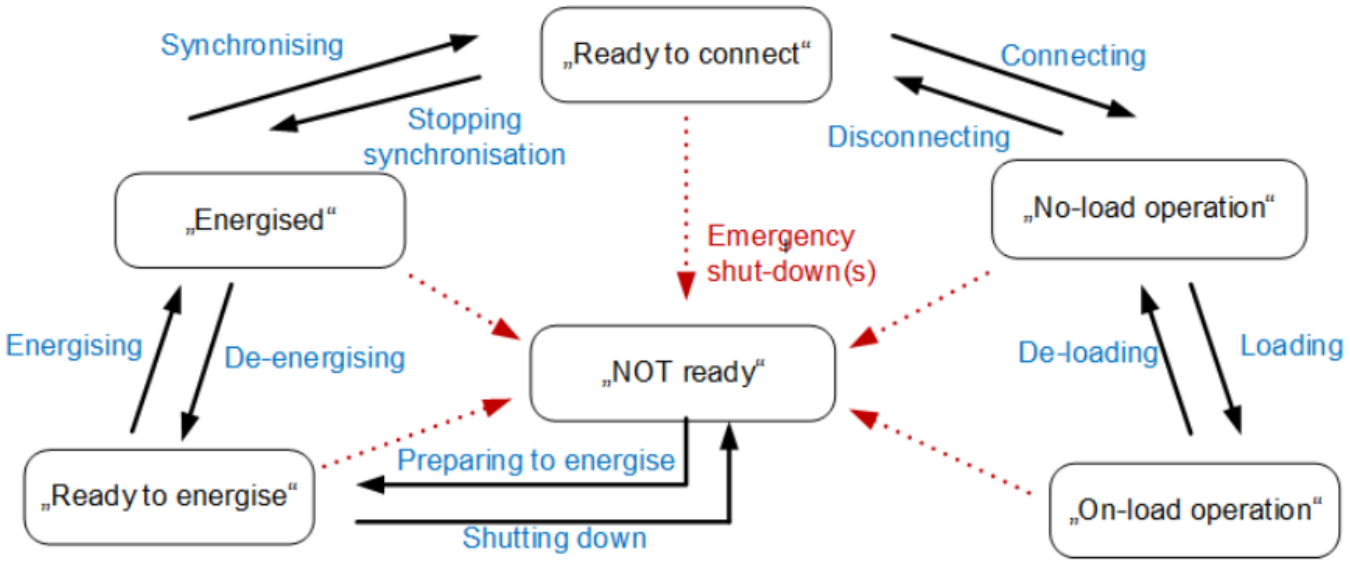


Figure 159: Operating states and transitions for AC/DC converter stations, as introduced in CENELEC

The CENELEC standards specify the following operating states and the associated transitions for AC/DC converter stations.

Operating state	**Definition (from CENELEC standards)**
“Not Ready”	Converter is disconnected from all energy sources
“Ready to energize”	All systems necessary to be energized are ready and internal communication is active
“Energized”	From AC: connection to AC side is made and AC voltage is established From DC: Desired DC voltage is established from the transmission path and DC voltage is controlled
“Ready to connect”	To AC (after energization from DC): Converter AC voltage is synchronized with voltage at PoC AC To DC (after energization from AC): Converter DC voltage is synchronized with voltage at PoC DC
“No load operation”	Initial set point remains at 0 MW and 0 MVAr
“On load operation”	

Several observations should be made regarding this nomenclature

- **Controlled and uncontrolled energization** steps are not differentiated. Those two steps are however very different and should be treated distinctively.
- The transition between the “energized”, “Ready to connect” and “no load operation” states may be different than suggested in CENELEC diagram. It is for instance possible that several interconnected portion of the HVDC grid are simultaneously energized in blocked state. This would make the AC/DC converter “connected” to neighboring lines or converters, but the DC voltage would not be controlled to its nominal value.
- Some operating step will differ significantly between offshore and onshore converter stations. The following is assumed:
  - Offshore converter station can only be energized from DC side.
  - Offshore converter station is responsible for the control and “forming” of the AC offshore grid, which is how the “ready to connect” state should be understood in case of energization from DC side.
  - Onshore converter station can be energized from AC or DC side.
  - Onshore converter station can be synchronized to AC onshore grid or, for instance in the context of black start, control the offshore AC voltage.

It is thus proposed to divide the “energized” state into a “blocked and energized” state, and a “de-blocked and energized” state. In addition, the possibility for a converter to go directly from “deblocked and energized” to “no-load operation” is added, if the AC/DC converter is already connected to other HVDC grid installations. The configuration of a blocked converter already connected to an HVDC grid also occurs in normal operation when a fault leads to the blocking of a converter. This converter will be deblocked while remaining connected to the rest of the HVDC grid.

A modified version of the diagram of operating states and sequences is proposed in Figure 160. For the sake of clarity, only the “start-up” sequences have been shown, the “shut down” can be directly deduced from Figure 159.

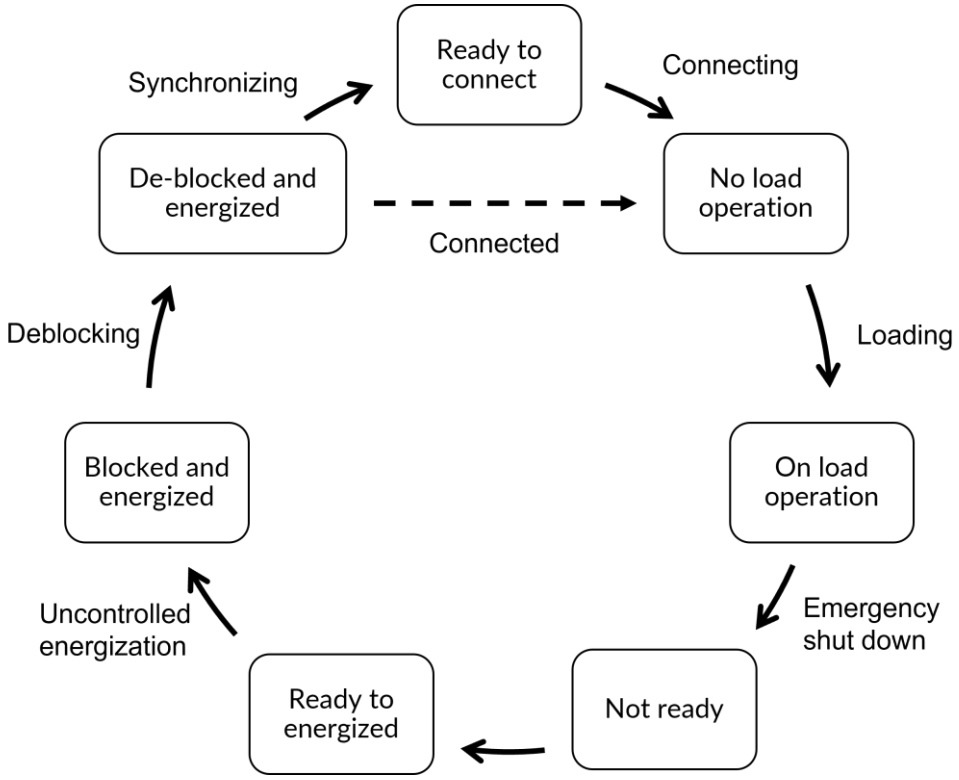


Figure 160: Proposed modified operating states and transitions for AC/DC converter stations. The "energized" state has been divided into "blocked and energized" and "de-blocked and energized" states. The possibility of a converter already connected to other HVDC grid installations has been added

Operating state	**Definition (modified)**
"Blocked & energized"	From AC: connection to AC side is made and AC voltage is established From DC: the desired DC voltage is established from the transmission path
"De-Blocked & energized"	Submodules are charged to the nominal DC voltage and converter can operate in one of the available control modes

Operating states will be put into practice by studying different start-up scenarios. The focus is intentionally put on the start-up of the meshed HVDC grid. The start-up of the wind-farms and the power ramp-up are thus left outside the following studies. Different start-up sequences are proposed and compared, with the goal to assess the possibility of starting the HVDC grid in various configurations. The topology of use case 1 and 2 are reproduced in a simplistic test benchmark using AVM-DC models in blocked and deblocked states. The accuracy of the STB is first compared with the full PSCAD use case implementation.

The considered start-up sequences are divided into three categories, corresponding to different rationales

- Start-up of the whole HVDC grid (start-up A1, A2, and A3, using topology of use case 1)
- Start-up of the grid as individual point-to-points and then connection as an MTDC (start-up B1 and B2, using topology of use case 1)

- Start-up of the HVDC grid considering that some of the onshore AC converters are unavailable and that some onshore stations must be energized from the DC side. (Startup C using topology of use case 2)

The start-up sequences under study are summarized in Table 77. The specific steps of each start-up sequence will be further detailed in the following sections. The main questions and expected answers associated to each start-up sequence are formulated.

Table 77: Start-up sequences considered using STB

Start-up ID	Main steps	Related questions and expected findings
SU_A.1	Uncontrolled energization of DC grid already connected, simultaneous control of all MMC onshore, and sequenced deblocking of offshore MMC	This is the reference sequence implemented in the use case.
SU_A.2	The DC grid is energized in blocked state but each element (onshore station, spokes; offshore stations, and interconnectors) are energized one after the other. Control of DC voltage and deblocking of offshore stations is performed last.	Is it beneficial to energize in blocked state step-by-step or all at once?
SU_A.3	Identical sequence as SU_A.2 but offshore stations are deblocked simultaneously.	What is the impact of deblocking the offshore station at the same time?
SU_B.1	Each hub is first energized as a point-to-point link. The DC voltage is then controlled. The interconnector is connected last to form the MTDC grid.	Is it possible or beneficial to use the point-to-point configurations as an intermediate step during the start-up?
SU_B.2	As SU_B.1 but the onshore stations are deblocked as soon as possible, i.e. the hubs are energized from controlled onshore stations. The interconnector is also connected last.	Is it beneficial to energize DC subsystems from a controlled rather than from an uncontrolled onshore station?
SU_C (topology of use case 2)	The MTDC is energized using only two (out of four) onshore stations. The remaining two onshore stations are then energized from the DC side.	What is the impact of starting-up the grid with some onshore stations unavailable? What is the impact of energizing onshore stations from the DC side?

9.2.2. STB: Simplified start-up sequences

Simplified start-up sequences are implemented using the modeling elements presented in Section 3, with in particular the blocked MMC models for energization from both AC and DC sides, as well as the simplified AVM DC model, which are both reminded in Figure 161. The transition from the blocked to deblocked MMC models is further detailed.

For onshore MMC, the transition is mainly driven by the activation of the voltage control, which will control the DC voltage to its nominal value. For the offshore MMC, the voltage of the submodules is ramped up to reach the nominal voltage by inserting fewer and fewer submodules, compared to the blocked state where all submodules are inserted. Offshore MMC do not contribute to the DC voltage control and can thus be considered as passive elements during this step.

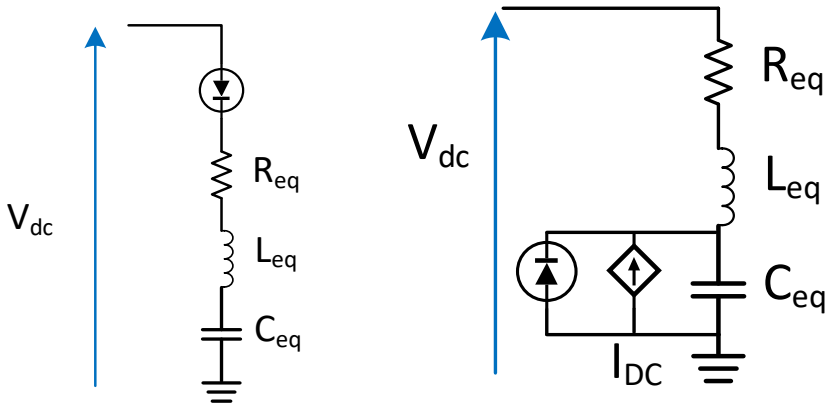


Figure 161: Average DC Model for blocked (left) and deblocked (right) energization

For the offshore converters, no current is injected (as we focus here on no load condition), and the AVM model amounts to an RLC circuit.

The transition from the blocked to the controlled states of the converter is done differently for onshore and offshore converters.

→ For onshore converters, the blocked model is disconnected and the deblocked model is connected at the same time. To account for the partial energization of submodules, the equivalent capacitor in Figure 161 is initially charged at $V_{blk} \simeq 420$ kV.

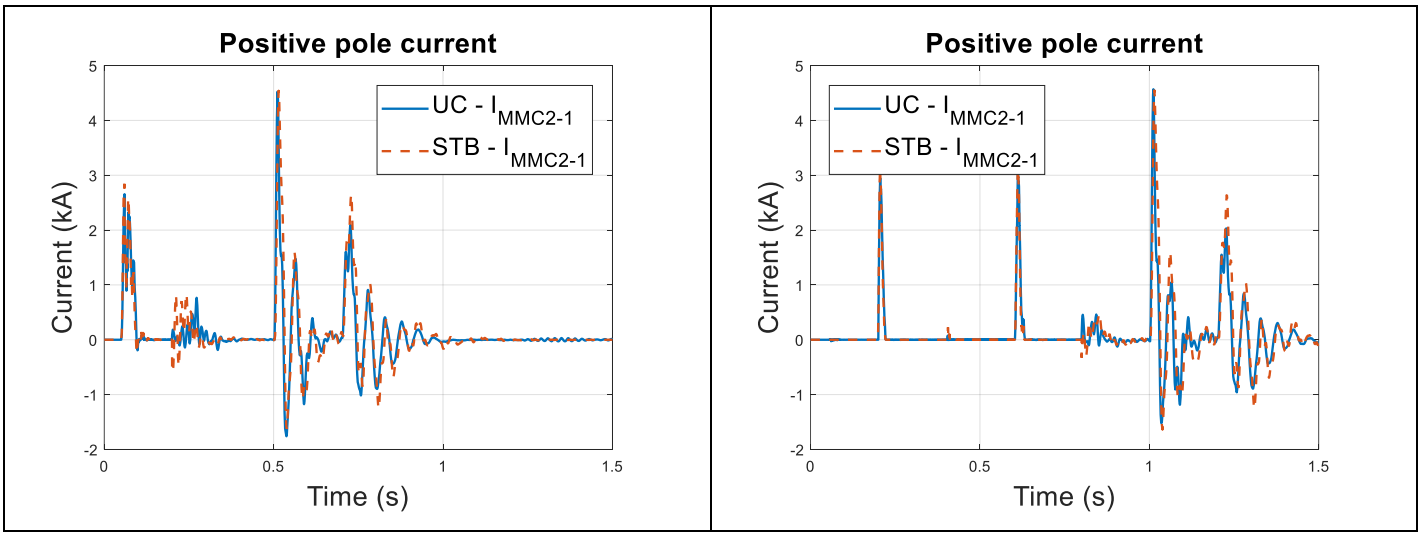
→ For offshore converters, at the deblocking of the converter, the number of inserted submodules in each arm is decreased. Consequently, the equivalent total capacitor of the RLC model is increased. If submodules are removed instantaneously, this change in the capacitor value will also be instantaneous, leading to an important inrush current. Alternatively, the submodules can be removed progressively. From the perspective of the AVM model, this amounts to a ramp up of the equivalent capacitor from C_{arm} to $6C_{arm}$. The ramp up time was set to 15 ms to match the observed behavior in the full PSCAD model. This energization strategy is for instance used in [31] as an effective way to reduce the current stress during the deblocking.

The parameter ranges determined for pre-insertion resistor are employed, as specified in the following table. An AC side PIR of 25 Ohms, as specified in the input list file, was also included. The applied insertion time is always 50ms. Finally, the DCR considered in the grid is 0.1H.

Onshore AC side PIR	25 Ohms
PIR of spoke at both ends (long cable)	50 Ohms
PIR of interconnector at both ends (short cable)	100 Ohms
PIR for offshore MMC	40 Ohms

9.2.3. STB Start-up: validation

The previously introduced STB is validated with use case 1.1. Note that the proposed STB is non-generic and that the entire MTDC grid topology must be implemented (4 converter stations, 3 cables). The considered start-up sequences for validation are the start-up A1 and A2, detailed in Table 78 and Table 79. For those two sequences, the current at the output of the MMC2-1, the voltage at the extremity of L2 on the onshore side, and the voltage at the offshore PoC-DC are compared between the use case and the STB in Figure 162. It appears that the overall behavior during the start-up is quite well represented in the STB, though significant difference with the use case still exists. Those differences are somewhat larger after the DC grid voltage is controlled (t = 0.2s in SU-A1 and t = 0.8s in SU-A2) than during the uncontrolled charging process. This reflects the difficulty to obtain a simple yet accurate representation of the voltage control of the MMC. The peak voltage and current during the controlled energization of the offshore MMC (t = 0.5s & 0.7s in SU-A1 and t = 1s &1.2s in SU-A2) are still quite well accounted for. Overall, the STB is deemed accurate enough to be used as a comparison tool between different start-up sequences.



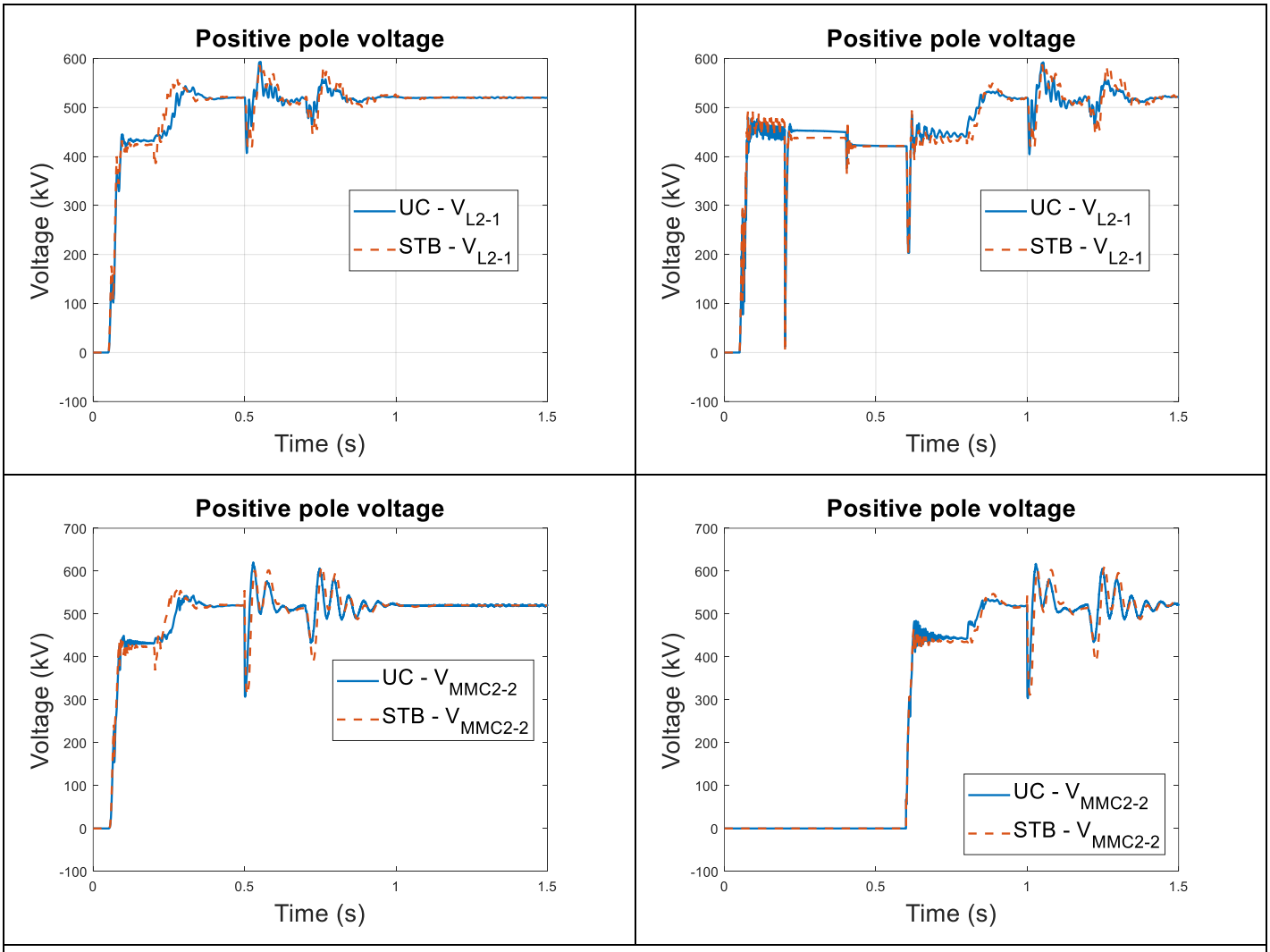


Figure 162: STB validation for start-up using use case 1.1. Left: start-up sequence A1, Right: start-up sequence A.2

9.2.4. Start-up sequences – uncontrolled grid energization

In this section, the start-up of the DC grid as a whole is considered through three different start-up sequences. The impact of controlling the DC voltage before or after the energization of part of the grid is investigated (scenarios SU-A1 and SU-A2). The impact of deblocking offshore stations simultaneously is evidenced in scenario SU-A3. Scenario SU-A1 corresponds to the standard start-up, where the DC grid is energized in blocked state all at once after the closing of the AC breakers. The onshore converter stations are then controlled, and the offshore stations are deblocked one after the other. The scenario SU-A2 proposes a sequenced start-up where DC subsystems (cables and offshore stations) are energized one after the other. The DC grid voltage is then controlled similarly to SU-A1. Scenario SU-A3 is identical to SU-A2 except that offshore stations are energized simultaneously. The detailed sequences of all three scenarios are provided in Table 78, Table 79, and Table 80.

Table 78: Start-up sequence for scenario SU-A1

Startup sequence SU-A1	**Time**	**Main behavior**
Closing of AC breakers, DC breakers and switches already closed	0.05	Uncontrolled energization of the entire DC grid
Deblocking of MMC onshore	0.2	DC grid voltage rises to the nominal value and is controlled
Deblocking of MMC offshore 1	0.5	
Deblocking of MMC offshore 2	0.7	

Table 79: Start-up sequence for scenario SU-A2

Startup sequence SU-A2	**Time**	**Main behavior**
Closing of AC breakers	0.05	Uncontrolled energization of onshore MMCs
Closing of DCCB and switches of spokes	0.2	Uncontrolled energization of both spokes
Closing of DCCB of interconnector	0.4	Uncontrolled energization of interconnector
Closing of disconnector switches of MMC offshore	0.6	Uncontrolled energization of both offshore MMC
Deblocking of both MMC onshore	0.8	DC grid voltage rises to the nominal value and is controlled
Deblocking of MMC offshore 1	1	
Deblocking of MMC offshore 2	1.2	

Table 80: Start-up sequence for scenario SU-A3

Startup sequence SU-A3	Time	Main behavior
Closing of AC breakers	0.05	Uncontrolled energization of onshore MMCs
Closing of DCCB and switches of spokes	0.2	Uncontrolled energization of both spokes
Closing of DCCB of interconnector	0.4	Uncontrolled energization of interconnector
Closing of disconnector switches of MMC offshore	0.6	Uncontrolled energization of both offshore MMC
Deblocking of both MMC onshore	0.8	DC grid voltage rises to nominal value and is controlled
Deblocking of MMC offshore 1	1	
Deblocking of MMC offshore 2	1	

Due to the symmetry of use case 1.1 and of the considered start-up sequences, only the current and voltage for MMC2-1 and MMC2-2 are detailed. The voltage at the onshore and offshore PoC-DC as well as the current at the output of the onshore MMC are provided in Figure 163, Figure 164, and Figure 165. Note that a given event (e.g., spoke energization) typically occurs at different times for the three scenarios. Some key observations are

- → The uncontrolled energization of the whole DC grid in one step (SU-A1) does not cause higher surge currents or larger voltage variations, compared to a sequenced energization (SU-A2).
- → The main inrush current and over/under-voltage occurs during cable energization and offshore station deblocking.
- → Simultaneous deblocking of offshore converters induces higher overcurrent (up to 7 kA) and should be avoided. The same start-up sequence performed with the detailed use case shows that this may even cause instabilities.

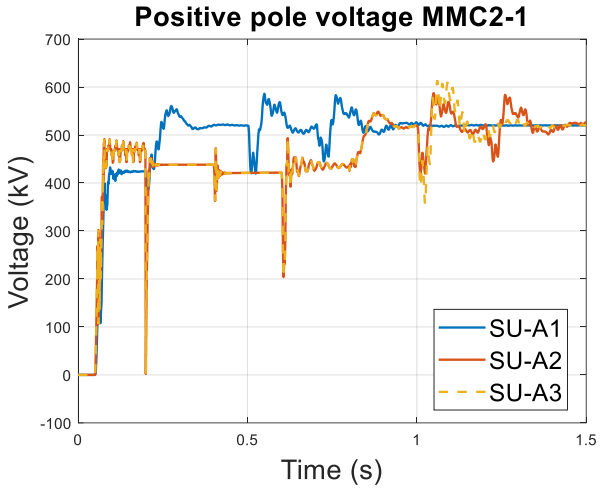


Figure 163: Comparison of onshore voltages during start-up for three different scenarios, using STB

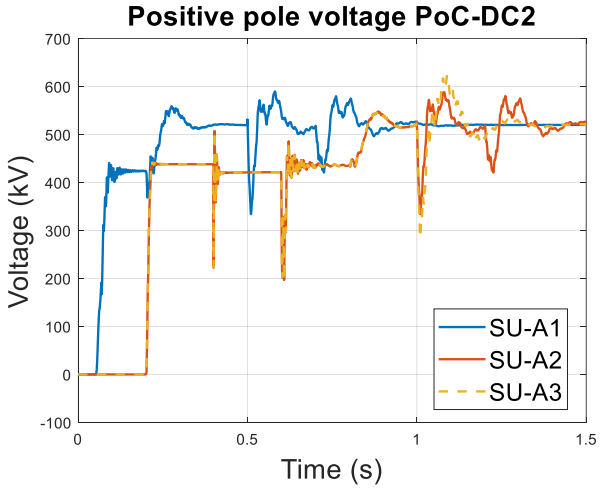


Figure 164: Comparison of offshore voltages during start-up for three different scenarios, using STB

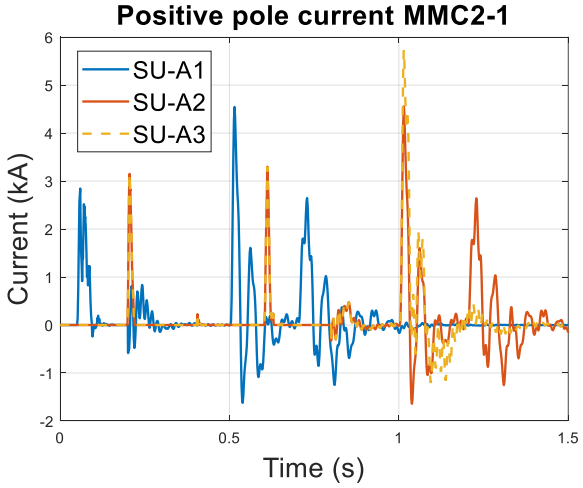


Figure 165: Comparison of onshore currents during start-up for three different scenarios, using STB

9.2.5. Start-up sequences – controlled grid energization

In this section, two alternative start-up sequences are investigated, where each hub is energized individually as a PtP before they are interconnected. In SU-B1 the DC voltage is controlled after the offshore stations and the spoke have been energized, while in SU-B2, the onshore MMC are deblocked before the hubs are energized. In both cases, the interconnector is connected in a last step. The voltage at the onshore and offshore PoC-DC as well as the current at the output of the onshore MMC are provided in Figure 166, Figure 167, and Figure 168Figure 165. As in the previous section, a given event (e.g. spoke energization) typically occurs at different times for the two scenarios. It is significant that in both scenarios, a large current surge (up to 6 kA) is observed at the deblocking of the offshore stations (0.8s), larger than the overcurrent observed in the start-up A1 and A2 in Figure 165. This can be explained as, in the two scenarios under study, the offshore converter capacitors are energized from a single onshore station through a spoke, whereas in the scenarios presented in the previous section, the inrush current was distributed between the two onshore stations. The start-up of the DC grid as multiple separate PtP appears thus as a more demanding scenario, though possible, than the start-up of the entire interconnected DC grid.

Furthermore, it appears that the uncontrolled energization of cables and offshore stations (SU-B1) induces smaller transients than the early control of the DC voltage through the deblocking of the onshore converters (SU-B2). In sequence B2, the blocked offshore MMC is energized while the onshore converter tries to maintain the DC voltage at its nominal value. The observed voltage oscillations are thus a downside of the control objective of the onshore converter that intends to actively control the voltage. By contrast in sequence B1, the onshore converter itself is blocked and the circuit is thus passive. Oscillations are not sustained.

Table 81: Start-up sequence for scenario SU-B1

Startup sequence SU-B1	**Time**	**Main behavior**
Closing of AC breakers	0.05	Uncontrolled energization of onshore MMCs
Closing of DCCB and switches of spokes	0.2	Uncontrolled energization of both spokes
Closing of disconnector switches of MMC offshores	0.4	Energization of both offshore blocked MMC
Deblocking of both MMC onshore	0.6	
Deblocking of both MMC offshores	0.8	DC voltage in both PtP rises to the nominal value and is controlled
Closing of interconnector	1	Energization of interconnector

Table 82: Start-up sequence for scenario SU-B2

Startup sequence SU-B2	**Time**	**Main behavior**
Closing of AC breakers	0.05	Uncontrolled energization of onshore MMCs
Deblocking of both MMC onshore	0.2	The DC voltage the output of both onshore MMC is controlled
Closing of DCCB and switches of spokes	0.4	Energization of both spokes
Closing of disconnector switches of MMC offshore	0.6	Energization of both offshore blocked MMC
Deblocking of both MMC offshores	0.8	
Closing of interconnector	1	Energization of interconnector

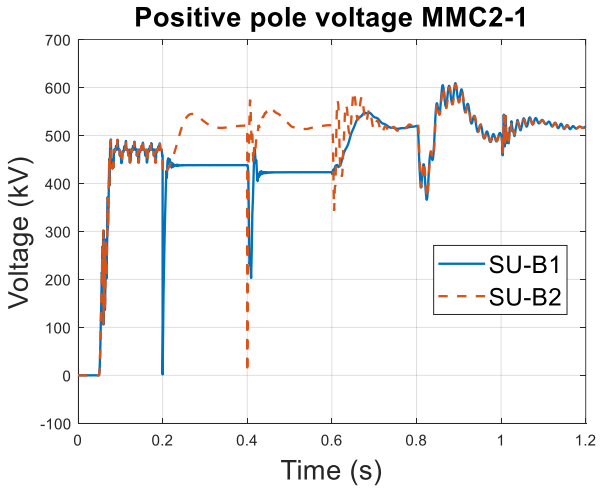


Figure 166: Comparison of onshore voltages during start-up for two different scenarios, using STB

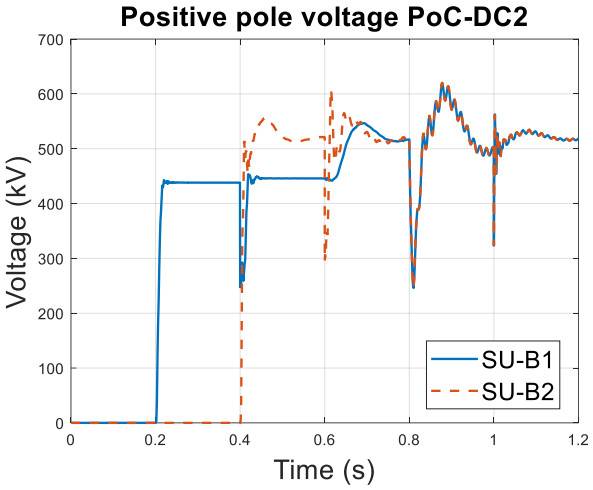


Figure 167: Comparison of offshore voltages during start-up for two different scenarios, using STB

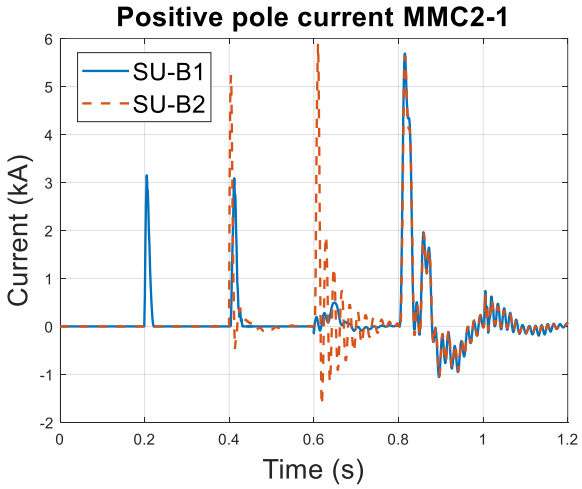


Figure 168: Comparison of onshore currents during start-up for two different scenarios, using STB

9.2.6. Start-up sequences – onshore station unavailability

In this section, the ability to start-up the grid using only some of the onshore converter stations is investigated using use case 2. Such a configuration is particularly relevant in two situations

- → Start-up of the DC grid while some of the onshore stations are out of service
- → Start-up of the DC grid from some of the onshore stations and energization of the remaining onshore stations from the DC side, as part of a DC black-start

Those two situations are evaluated simultaneously using the start-up sequence in Table 83. The entire grid is energized starting from stations 1 and 2. The spokes 3 and 4 are disconnected. The four offshore stations as well as the interconnectors are thus energized from only two onshore stations, with the two remaining onshore stations disconnected. The converter stations are then deblocked, starting from the onshore. This first stage represents a degraded start-up where some of the onshore stations are unavailable.

Once the DC voltage is controlled, the spokes 3 and 4 are closed and the MMC3-1 and MMC4-1 are energized from the DC side, and then deblocked. This second stage accounts for the ability of the DC grid to energize some of the onshore stations from the DC side, typically as part of a DC black-start. The logical next step that would consists in the control of the onshore AC voltage by the MMC3-1 and MMC4-1 requires more complex control and modeling that are out of scope of this study. The topology of use case 2 is replicated using simplified models, as for use case 1.1. The start-up sequence is simulated with the STB and UC and compared, except for the last step (control of MMC3-1 and MMC4-1) which is only performed in the STB as the DC side controlled energization for onshore station is not available in the implemented use case and requires development.

Table 83: Use case start-up sequence representing the energization of the MTDC grid using only two onshore stations, and energization of remaining onshore stations from DC side

Startup sequence SU-C	**Time (s)**	**Main behavior**
Closing of AC breakers 1 and 2	0.1	DC grid uncontrolled energization
Deblocking of onshore MMC1-1 and MMC2-1	0.4	DC grid voltage rises to the nominal value and is controlled
Deblocking of offshore MMC2-2 and MMC3-2	0.7	
Deblocking of offshore MMC1-2 and MMC4-2	1	
Connection of spokes L3 and L4	1.3	Spokes and MMC3-1 and MMC4-1 are energized
Deblocking of onshore MMC3-1 and MMC4-1	1.7 & 2	

The voltage and current evolution of onshore and offshore stations are shown in Figure 169. As for the previous start-ups, the STB allows to represent the overall behavior of the voltage and current during the start-up, though its accuracy decreases after the DC voltage control is activated (t = 0.4s). The simple blocks used in the STB allow to easily investigate the deblocking of the onshore stations MMC3-1 and MMC4-1 (at t=1.7s and t=2s). It is significant that the start-up of the entire DC grid comprising 4 offshore stations with only 2 onshore stations does not raise any particular issue.

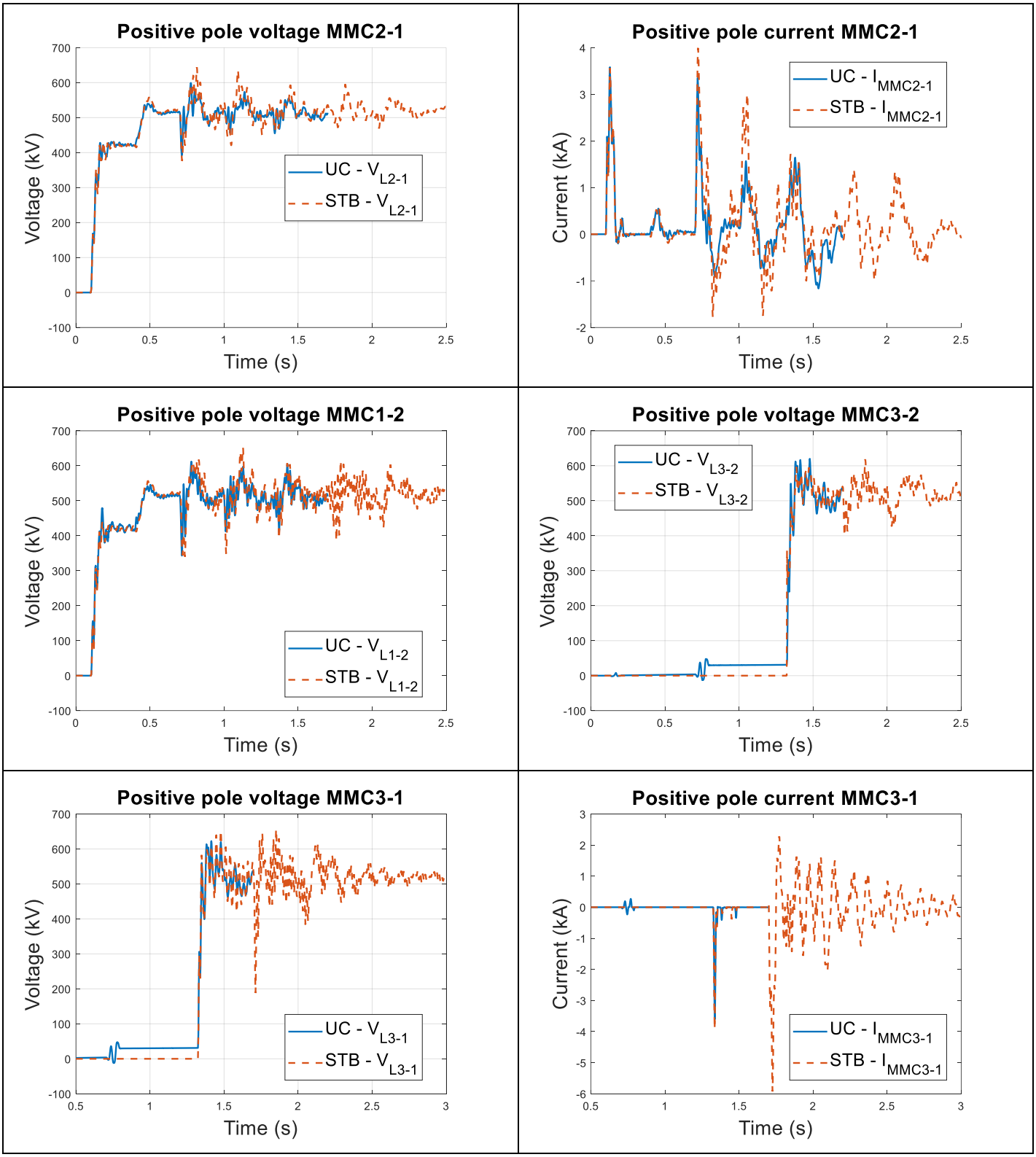


Figure 169: Voltage and current of UC2 and STB during the start-up of the meshed grid using only MMC1-1 and MMC2-1. DC voltage is controlled at t = 0.4s, and offshore stations at t=0.7s and t = 1s. The spoke 3 and 4 and connected onshore stations are energized at t = 1.3s

9.2.7. Main conclusions

In this section, the start-up of the grid in various configurations has been investigated using UC1.1 and UC2. An STB has been developed to represent the main behavior during the grid start-up. It was found that the grid can be start-up using various sequences controlling the DC voltage at an early or a late stage. The energization can be also performed in a sequential manner – energizing each cable/converter individually – or simultaneously. The particular case of the energization of the grid as individual point-to-points was also demonstrated.

The main **critical step is the deblocking of the converters charged from the DC side (typically offshore converters) that induces a large inrush current and voltage oscillations**. This inrush current can lead to sustained oscillations in the DC grid if, for instance, nearby offshore converters are deblocked simultaneously. It is thus recommended that the two offshore converters are deblocked sequentially, one after the other.

The inrush current at the deblocking of a converter energized from the DC side can be limited by applying an adequate control of the modulation index. The number of inserted submodules can then be smoothly ramped down which avoids the surge of the submodule voltages. An additional option is to force the insertion of a resistor, though no circuit breaker is normally operated during the deblocking.

Finally, the start-up of the grid from a reduced number of onshore converters was investigated. This scenario shows the possibility to start up the grid with some converters unavailable. The energization of the remaining onshore converters from the DC side also shows the possibility to perform DC black start, which energizes the onshore stations through the DC grid.

ID	Functional requirement
Master_Control13	The DC grid controller should be able to perform different sequences to start up the DC grid, depending on the availability of the HVDC grid installations. The transient voltage and current during the start-up should be limited to acceptable values.
On_ACDC_Con12	It should be possible to energize the onshore converter stations from both the DC and the AC sides.
General71	The inrush current caused by the deblocking of a converter energized from the DC side should be limited to predefined acceptable values.

9.3. Switchgear requirements

The generic configuration of switching station connecting a converter station by multiple cables is reminded in Figure 170, adapted from CENELEC and [14]. A grounding unit is proposed, gathering two grounding options: a solid grounding (through small impedance Z) and a non-solid grounding through a surge arrester.

The main HVDC switchgear in an DC switching station are listed in Table 84, reproduced from [14]. For the sake of clarity, the switchgears within the converter units are omitted. The circuit breaker is intentionally omitted as it is addressed thoroughly in the functional group protection. Switching equipment is classified into “disconnecting switches”, “earthing switches”, and “transfer switches”. Note that some earthing switches are under “transfer switch” when their main duty consists in transferring current. Disconnecting switches are generally used to interrupt small residual currents.

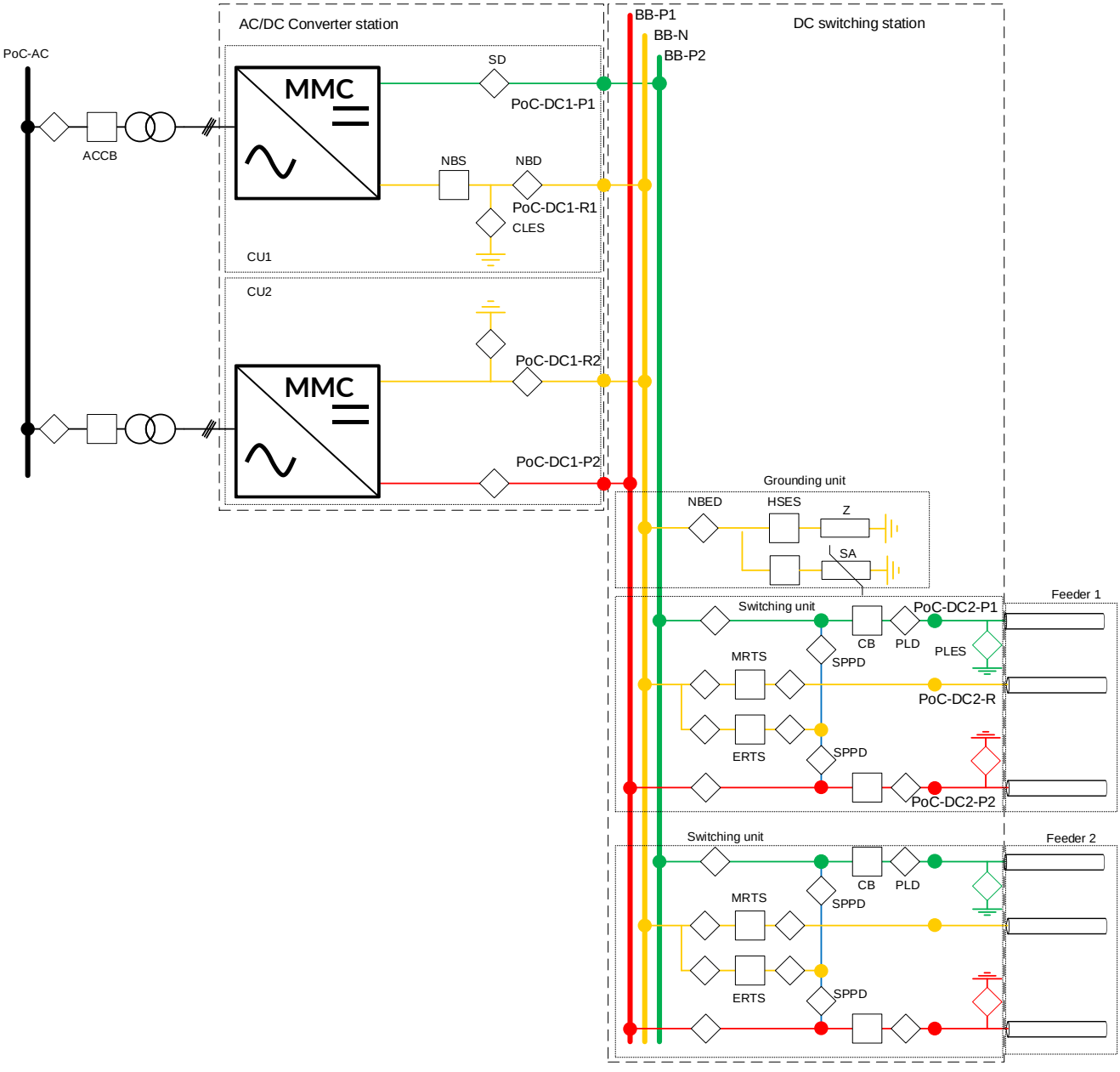


Figure 170: Diagram of a generic switching station connecting a converter station and two feeders

Table 84: Main DC switching equipment in HVDC switching station, from [14]

Acronym	Full name	Main duty	Details
Disconnecting switches			
SD	Substation Disconnecting Switch		Isolation of the high-voltage side of a substation pole from the line for maintenance
LD	Line Disconnecting Switch		Open line in the absence of DCCB, see spoke disconnection
PLD	Pole Line Disconnecting Switch		
NBD	Neutral Bus Disconnecting Switch		Isolate the neutral end of a substation pole
NBED	Neutral Bus Earthing Disconnecting Switch		Isolate the high-speed earthing switch (HSES) for maintenance
SPPD	Substation Pole Paralleling Disconnecting Switch		Paralleling the substation poles after a polarity reversal has been performed in one of the poles
Earthing Switches			
PLES	Parallel Line Earthing Switch	Earthing Withstand voltage	Earthing of the pole line, incl. cable discharge
PPES	Parallel Pole Earthing Switch		Earthing of one or both HVDC pole line(s), e.g. for maintenance
SES	Substation Earthing Switch		Earthing of the substation
Transfer switches			
HSES	High Speed Earthing Switch	Commutate current Making current Withstand voltage	Provide solid grounding Transfer ground current to neutral path
NBS	Neutral Bus Switch		Closed in normal operation

			Commutate the current away from the pole in case of converter blocking
MRTS	Metallic Return Transfer Switch		Clear metallic return fault
ERTS	Earth Return Transfer Switch		Connect HV as neutral path

9.3.1. Disconnecting switches

The specification of disconnecting switches from existing projects and literature as described in [14] is deemed precise, sufficient, and applicable to MTDC projects.

One exception is the specification of the Pole Line Disconnecting (PLD) switches which, in the absence of DCCB (e.g. at the onshore side), should be able to open a pole after the current has been interrupted by the tripping of DCCB, or by control action. An example of such a scenario is provided in Section 7.1.4. The results show that the currents to be interrupted is within 1-10A and presents 0-crossings, with a TRV of tens of kV, see Figure 171. The performances of existing HVAC DS seem thus sufficient.

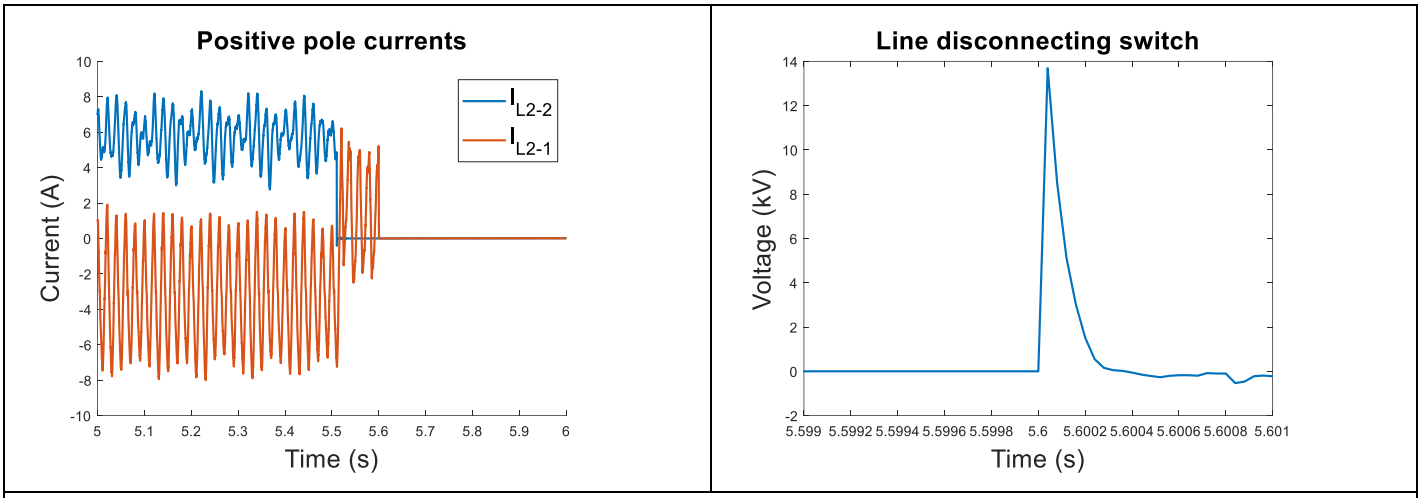


Figure 171: Typical duty of line disconnecting switch after the unloading of a line and the operation of the opposite side DCCB (t = 5.5s). Results are taken from the spoke disconnection sequence detailed in Section 9.1.4

9.3.2. Earthing switches

As for disconnecting switches, the specification of earthing switches in [14] is deemed precise, sufficient, and applicable to MTDC projects. The need for a discharge resistor in series with the pole line earthing switch is further investigated.

The main function of the pole line earthing switch (PLES) is to earth the pole line. If trapped charges are present, the PLES must be able to discharge the pole while avoiding high overcurrent and voltage polarity reversal at the remote end. The discharge phenomenon of a cable closing into a resistor can be represented by a simple STB comprising a pi-section cable. Depending on whether DCR are between the discharge switch and the cable or not, they should be included in the STB, as presented in Figure 172. The cable discharge behavior in the two

cases is presented in Figure 173 and the pi-section model is compared with a wide-band model for a 200km cable. The use of the pi model is validated. The location of the DCR between the discharge switch and the cable significantly changes the behavior: without the DCR, the propagation of the TW is the dominant phenomenon, while with the DCR, the cable discharge amounts to a classical RLC circuit.

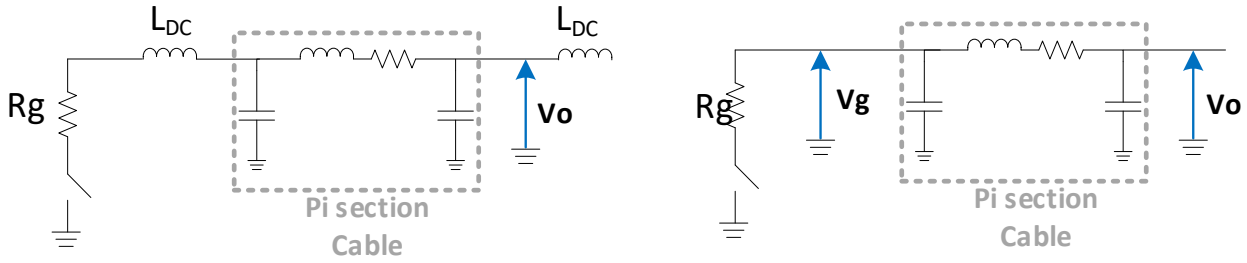


Figure 172: STB for sizing of cable discharge resistor with (left) and without (right) DCR between the discharge switch and the cable

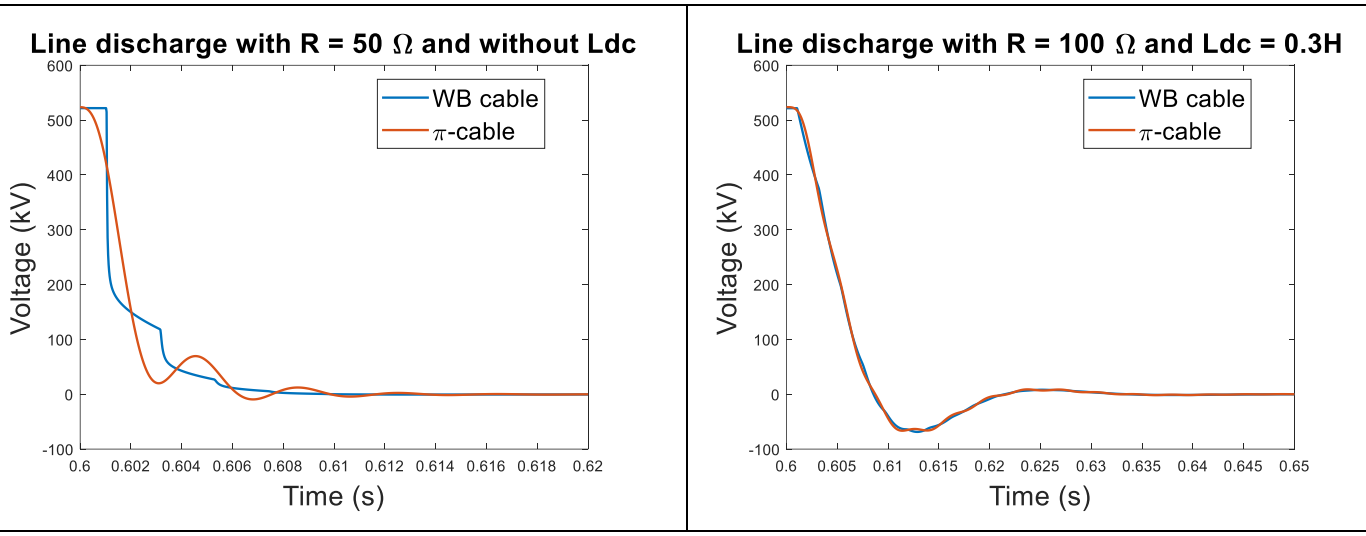


Figure 173: Voltage at the open end depending on the DCR location, and with a wideband cable and pi-cable model

If no DCR is included in the circuit (i.e. the DCR is on the other side of the DCCB), the discharge transient can be studied analytically using traveling wave theory.

As the earthing switch closes, the initial voltage surge at the closing end is

$$V_g = \frac{-Z_c}{Z_c + R_g} V_n$$

Neglecting the attenuation due to the propagation along the cable, the voltage at the open end of the cable is

$$V_o = 2V_g$$

This first voltage wave should not induce a voltage reversal, i.e.,

$$V_n + V_o > 0$$

In the case where no DCR is included, this condition leads to

$$R_g > Z_c \simeq 40\Omega$$

If the DCR is in series with the cable, the transient behavior due to the propagation of traveling waves is no longer the dimensioning behavior. Instead, the RLC circuit formed by the cable, the DCR and the resistor can be oscillatory and cause itself a voltage reversal. A simple STB consisting of a pi-section for the cable, as presented in Section 3.1, is used to evaluate the required discharged resistor size to avoid voltage reversal depending on the cable length and the DCR size.

The required discharge resistor to avoid voltage reversal is evaluated with extensive simulations using the STB in PSCAD, see Figure 174. This configuration (DCR between the discharge switch and the cable) thus requires much larger discharge resistor than the configuration without DCR.

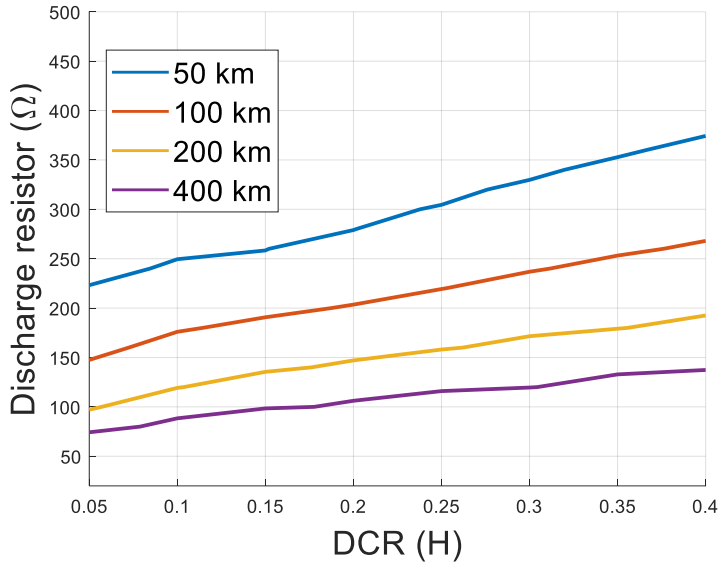


Figure 174: Required discharge resistor size to avoid voltage reversal for different cable lengths and DCR size

9.3.3. Transfer switches

The transfer switches are:

- The Metallic Return Transfer Switch (MRTS), which acts as the disconnector of the metallic return. The most demanding duty for the MRTS is the disconnection of the DMR in case of a fault. It was assumed in this case that enough time was available to rebalance the grid and thus unload the DMR before the opening of the MRTS. This scenario is investigated in Section 9.1.7, showing that a transfer capability of a few 10's A with a TIV of 30 kV is sufficient. Nevertheless, if the MRTS must be able to transfer the DMR current before the rebalancing of the grid, the transfer capability should be up to the nominal current. It should be emphasized that the possibility to transfer the DMR current is only possible if an available current path is available. The earth can provide such a path for a limited time. The use of an HV pole as DMR is another possibility.

- The Earth Return Transfer Switch (ERTS) allows to use one of the HV conductors as DMR, if necessary.

- The main purpose of the High-Speed Earthing Switch (HSES) is to act quickly in case of an overvoltage on the neutral bus to ensure the grounding of the HVDC system. In the context of multi-terminal HVDC grids, the role of HSES should be further specified.

A converter station may have multiple grounding options, one being a solid grounding (or grounding to a small resistance). In steady-state operation, one and only one station throughout the grid must be solidly grounded. The other stations are grounded so that earth current is not permitted, typically through a surge-arrester. The main goal of the HSES is thus to switch back and forth between the solid and non-solid grounding of the station. A slower switch should then be installed to allow the disconnection of the surge-arrester. The main duties of the HSES are

- → If opened, HSES should be able to close in case the grounding is lost in the HVDC grid or part of it.
- → In case of double grounding points in the grid, the opening of the HSES should transfer the ground current to the neutral path.

The reconfiguration sequence presented after a DMR fault in Section 8.1.7 requires both actions.

9.3.4. Conclusion

The functional requirements for DC switchgear investigated in this section are listed in the following table.

ID	Functional requirements
Off_SS10	The disconnector switches within the switching station (incl. SD, PLD, NBD) should be able to interrupt a residual DC current.
Off_SS11	The earthing switches within the switching station (incl. PLES, NBES, CES, SES) should be able to ground part of the HVDC installation that has been disconnected from any active source.
Off_SS12	The discharge of a disconnected cable should not induce a voltage reversal. A discharge resistor can be required to avoid such a behavior.
Off_SS13	The metallic return transfer switch should be able to disconnect the metallic return in case of DMR fault, in compliance with the chosen strategy after DMR fault.
Off_SS14	In case a solid grounding option is available at the switching station but not used, the HSES should be able to close in less than a specified time to ensure that the grid is effectively earthed.
Off_SS15	In case the switching station is effectively earthed, the HSES should be able to open and transfer the ground current to the neutral path.

10. Next Steps

→ MTDC Grid Control functional group

> Droop control schemes have not yet been standardized today and several possible candidate schemes have different characteristics. Investigations of the behaviors of different droop control schemes within the same DC grid is recommended to avoid DC control interoperability issues.

> The provided analysis for MTDC grid control have been performed using the so-called “Non-Energy Based Control”. Some conclusions may be different and require more investigations with other control structures such as Energy Based Control.

> investigations of DC reactor limits to avoid DC voltage instability issues should be investigated considering different droop control schemes.

> Tripping of certain OWF to support the containment of DC voltage excursion may be beneficial. However, given the speed of the DC voltage dynamics and the time required for the communication for detecting the rise and for sending the command + tripping of AC circuit breakers, it is still questionable whether the design of the parameters that affects the entire system can rely upon this solution. The feasibility and reliability of the solution requires further investigation.

> In-depth analysis of the influence of the post-contingency quasi-contingency DC voltage deviation on the internal parameters of the MMCs, such as the arm currents and the SM capacitor oscillation.

> Further investigation and parameter determination with sensitivity analysis considering all modes of the system using MIMO approach.

→ DC Protection functional group

> AC system criteria TS duration. More detailed analysis of frequency stability after DC fault could be carried out, for instance considering a multiple machine model instead of a single machine model. As pointed out in some commentaries, the definition of TS and PS in the context of multiple asynchronous zones could also be investigated.

> As mentioned within the report the design of protection components (DCR, DCCB operating time, etc.) does not only depend on the DC fault currents but also on DC-FRT over and undervoltages limits and their duration. Those limits and duration depend on several parameters like the system strength, power quality on the AC side, the MMC energy level but control modes and parameters also have an influence. In depth investigation of impact of such different parameters on the DC-FRT is recommended.

> The proof-of-concept through EMT simulation proved that the STB environment can be effectively employed for a preliminary design of DC protection components. Further investigations can be carried out for the development of STB considering different switching station topologies or possible extension of HVDC building blocks (i.e. considering more than one MMC installed within a switching station or more than two internal interconnectors or spokes).

> The sensitivity analysis regarding the impact of different parameters (MMC blocking criteria, MMC sub-modules energy, DCCB operating time, DC breaking capability, etc..) is carried out considering that the value of DC reactor is the same at each line end and at each MMC DC side output. A more detailed analysis considering optimization of DC reactor values depending on the DC reactor installation within the DC grid could bring different results.

> The impact of different operating times for the DC circuit breaker installed within the same grid could have a major impact on the future interoperability of DC grid protection and should deeply investigated.

> Within this study, a DCCB is proposed at the DC side output of the onshore MMC installed at the DK AC synchronous. Indeed, because the DK zone is supposed to be a weak system, it is chosen to maintain the MMC controllability (MMC blocking is not allowed) after a fault on the connected spoke. A fast blocking and deblocking of the onshore MMC converter could be investigated and, if the feasibility is confirmed, a relaxation of the design of the DC reactor and DCCB at the MMC output could be possible.

→ DC ancillary services functional group

> Within this report a DBS installed at the DC side is considered for ancillary service related to temporary power imbalance. Future investigations can be addressed to analyze possible advantages of AC chopper installed at the AC valve side of the offshore MMC converter, particularly in the case in which the AC sides of the offshore MMC bipole are coupled.

> The DBS operation simulation results in this report have been obtained by a detailed model with a chopping resistance. Other DBS topologies exist, and their performance could be further investigated. Beside of detailed performance investigation a simplified DBS model could be developed to narrow down design parameters (i.e. energy dissipation requirements, DBS activation functions, Harmonics injection, interaction with DCR…).

> The possibility to energize and start-up the DC grid from an offshore station was not considered, as no source of guaranteed source of energy was included at the offshore side (e.g. battery).

> The analysis of the black-start functionality was limited to the energization of the DC grid from some onshore station, and the energization of the remaining onshore stations from the DC side. Further investigation on the capability to control the onshore AC voltage would be relevant, typically based on grid-forming controls.

→ Operational regimes functional group

> Within this study hypothesis is taken to not operate the grid in rigid bipole after a DMR fault. The main reason for this choice is related to the management of neutral voltage reference, particularly when the grid is split in two zones because of the loss of the DMR connecting the two zones. To keep a reference voltage of the neutrals in this condition a particular converter control mode needs to be developed and studied. Operation of the grid with part of the network in rigid bipole configuration is considered to be feasible but requires more in-depth studies.

> The focus in this study was put on the energization steps. The de-energization and shut down of the DC grid or part of it could also be investigated.

> A detailed assessment of the communication requirements between the DC grid controller and local HVDC installations (switching stations, converter stations) would be relevant, for a complete overview of the requirements for the coordination of DC connection modes and operational modes.

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12.Appendix

12.1. Impact of DC faults on AC system stability

This section shows the calculation of the amount of loss of power during PS and TS for an HVDC building block considering different type of faults and based on the AC system criteria proposed in section 7.1. The methodology for the calculation is the same as reported in [32]. As a reminder, Figure 175 shows the failure rates and classification of faults depending on failure probability as well as the AC system criteria as considered in [32].

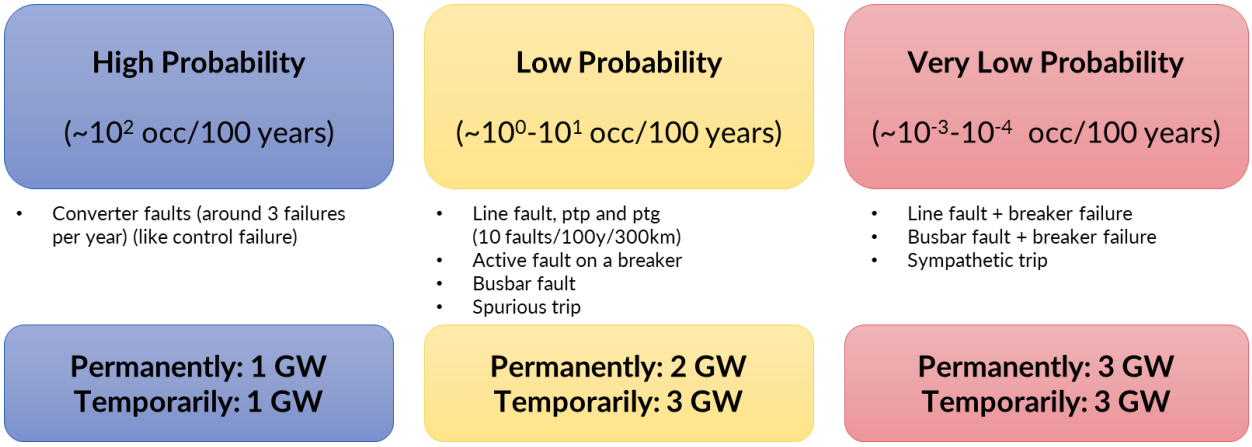

Figure 175: Classification of faults depending on failure probability and AC system Criteria proposed in [32]. Temporary Stop was initially assumed to last 150ms.

Table 85 shows the calculated loss of power (per pole) during PS and TS for an HVDC building block of 2 GW (per pole) considering the new AC system criteria proposed in in section 7.1. In blue are highlighted the values that change compared to the values calculated with the criteria presented in Figure 175. The busbar configuration is assumed to be a Double Bus Single Breaker (DBSB) configuration. It is also assumed that it is possible to reconfigure DC switches within 1-2 seconds.

For example, after a busbar fault, with a reconfiguration of the busbar within 2s, the TS requirement (2GW for 4s) is fulfilled, and the PS is therefore limited to 1 GW. For line fault ptp + breaker failure the PS is limited to 2 GW.

Table 85: Loss of power (GW, per pole) during PS and TS for 2 GW node HVDC building block

Probability	Fault types	DBSB configuration	
		TS[16]	PS
High	Converter failure	$1_{(PS)}$	1
Low	Line fault ptg	$1_{(PS)}$	1
	Line fault ptp	$2_{(PS)}$	2
	Busbar fault	$1+1_{(PS)}$	~~2~~ 1
	Active breaker failure	$1+1_{(PS)}$	~~2~~ 1
Very low	Line fault ptg + breaker failure	$1+1_{(PS)}$	~~2~~ 1
	Line fault ptp + breaker failure	$1+2_{(PS)}$	~~3~~ 2
	Sympathetic trip line fault ptg	$1+1_{(PS)}$	~~2~~ 1
	Sympathetic trip line fault ptp	$1+2_{(PS)}$	2
	Busbar fault + breaker failure	$2_{(PS)}$	2

It can be concluded that the new AC system criteria of TS duration of 4s (instead of previous value of 150ms)[17] combined with a requirement for DC switches reconfiguration within 1-2 s allows to reduce the PS requirement from 3 GW to 2 GW, which has an impact on need for FRR.

12.2. Sensitivity analysis on identification times

In this section the aim is to investigate how identification times impact the requirements on DC switchgear and DC reactors. The following identification times are considered:

- → Relay time: The relay time is the time between fault inception and sending the tripping order. It comprises the detection time and selection time according to [14]. Detection time is the time from fault inception to fault detection. The selection time is the time from fault detection to the decision which breaker should be tripped.
- → Breaker failure identification time: A breaker failure identification comprises several steps. First the failure needs to be detected by the DCCB that is supposed to open. Since the DCCB is supposed to hold the maximum TIV at the end of the operation time. Hence, failure identification can be supposed to be carried out

[16] The GW number in the TS column followed by the subscript (PS) means that the temporary stop is due to the permanent stop.
[17] Note that for the MMC connected to the wind farm (with assumption taken in [32]) a blocking of the converter entails an opening of the AC side wind turbine breakers and therefore a PS of the active power. Therefore, there is no allowed TS of the MMC connected to the wind farm.

without considering additional time. Secondly, the information needs to be sent out and treated by adjacent DCCBs. This time delay needs to be considered for breaker failure identification.

It should be noted that the detailed specification of time frames is out of scope. From a system level perspective, it is important to consider the overall delay that is imposed by fault identification and failure identification.

Figure 176and Figure 177 show the impact of different relay times on the operating time of the DCCB for a given i_{dcblk}=3pu. An increasing relay time results in a faster operating requirement for the DCCB. This is consistent since the DCCB operating time is the result of blocking time minus the relay time. The blocking time remains unchanged and thus the operating time needs to decrease.

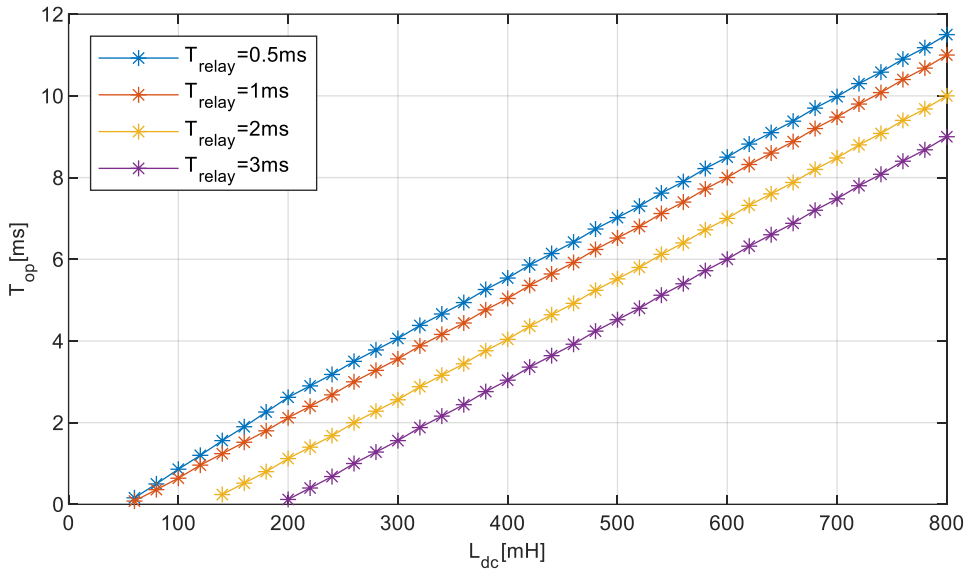

Figure 176 DCCB operating time requirements for different relay times; i_{dcblk}=3pu T_{relay}={0.5 1 2 3}ms

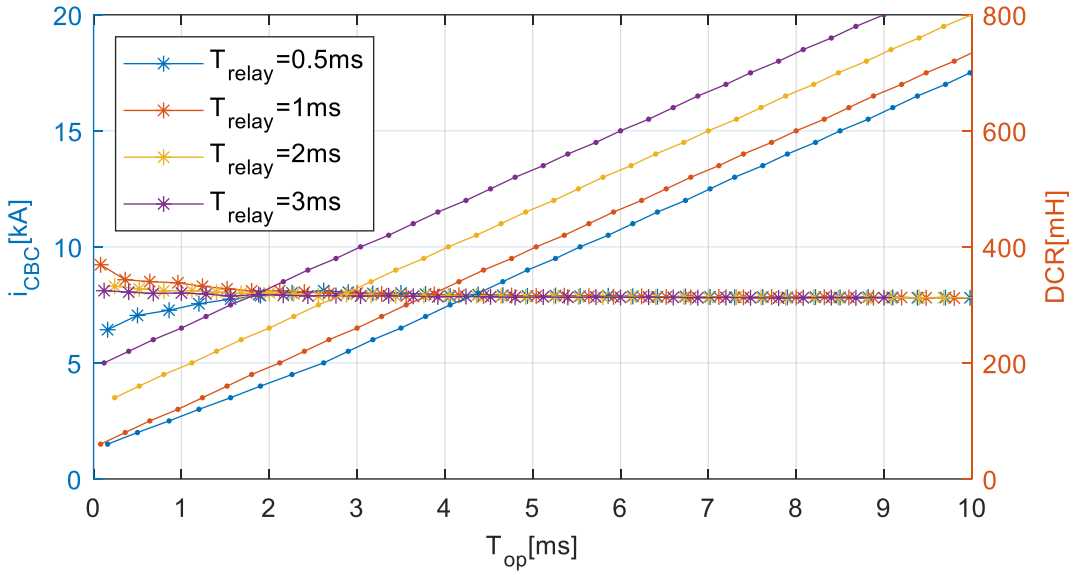

Figure 177 Current breaking capability and DCR requirements for different relay times dependent on the operating time; i_{dcblk}=3pu T_{relay}={0.5 1 2 3}ms. The left and right axis are linked respectively with 'star lines' (*) and 'dotted lines' (·).

The impact of a variation of breaker failure identification times is shown in Figure 178 . It should be noted that all cases where the results remain unchanged signify that the primary protection remains the dimensioning scenario. This is especially the case for high operating times since T_{BFI} is much smaller than T_{op}. For low operating times the increasing BFI time leads to higher DCR requirements for a given operating time. The decreasing requirement in terms of current breaking capability is a result of higher DC reactor value and hence slower increase of current.

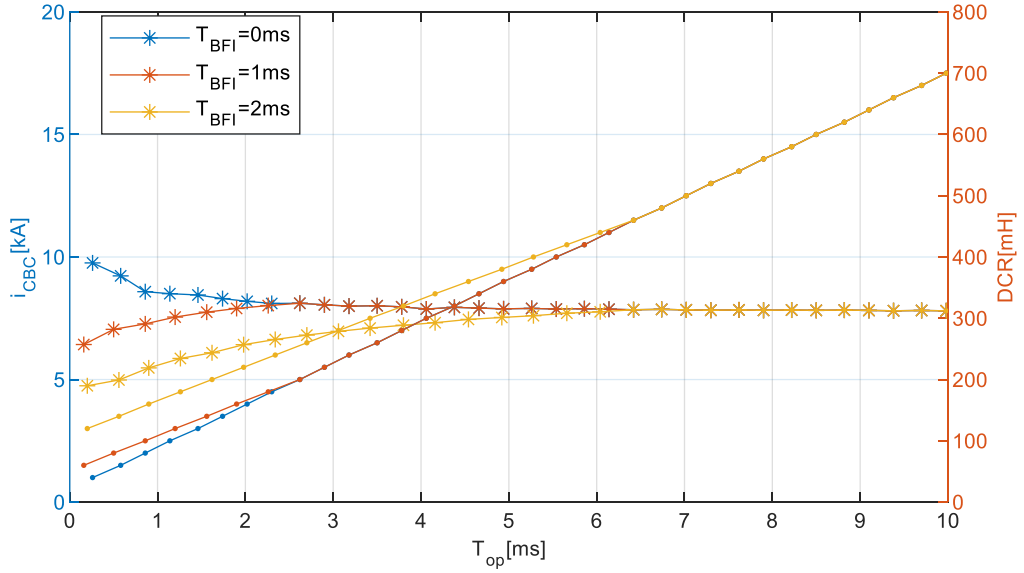

Figure 178 Current breaking capability and DCR requirements for different breaker failure identification times dependent on the operating time; T_{BFI}={0 1 2}ms, i_{dcblk}=3pu. The left and right axis are linked respectively with 'star lines' (*) and 'dotted lines' (·).

12.3. Dimensioning scenarios for DC protection specifications

The protection design as proposed in section 7.3 considers several fault scenarios and dedicated primary and backup protection sequences and dedicated blocking constraints (see Table 46):

- Busbar fault
- Line fault II
- Line fault spoke
- Line fault II + breaker failure
- Line fault spoke + breaker failure
- Line fault spoke + breaker failure onshore

The STB as proposed in section 7.3 consider a spoke fault as the dimensioning scenario. The following aspects are considered:

- A busbar fault is obviously electrically closer to the offshore converter (one DC reactor less between converter and fault compared to a spoke fault or II fault) but in case of a busbar fault the converter is not prohibited from blocking. The converter at the adjacent busbar is prohibited from blocking in case of busbar faults but three DC reactors are between converter and fault location against only two for spoke and II faults. Hence, spoke fault and II fault are dimensioning scenarios for DCCB operating time definition when considering equal DC reactors.
- The current breaking capability for a busbar fault is shared among several breakers around the busbar whereas for an II fault or a spoke fault the fault current is interrupted by a single breaker. In the proposed STB II are replaced by ideal voltage sources which represents the worst case of fault current contribution from adjacent parts of the grid.

Further, it could be argued that the STB only considers Pole-to-Ground (PtG) faults while the protection components should also cover Pole-to-Pole (PtP) faults. However, the proposed STB considers ideal grounding such that the loop of the fault current has no additional electrical elements in the loop of the return path. For PtP faults the loop includes twice the voltage (±525kV) but also twice of RLC elements of the MMC and the DC reactor. This leads to an identical rise of fault current for PtP faults compared to PtG faults.

In the following PtG and PtP fault are applied at the output of the converter (see Figure 179). The results are shown in Figure 180. In can be seen that the fault current evolution in pre-blocked state is identical due to the aforementioned electrical composition. After blocking, the fault current related to the PtG fault increases to a higher value due to a higher contribution from the AC grid. In fact, if positive and negative pole are connected to the same AC-PoC the short-circuit current is shared among both poles in case of PtP faults which leads to a lower fault current per pole.

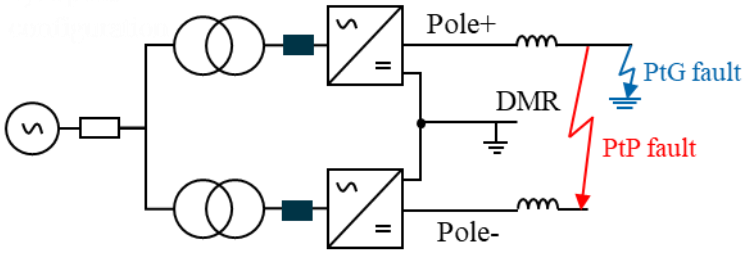

Figure 179 SLD for PtG and PtP fault comparison

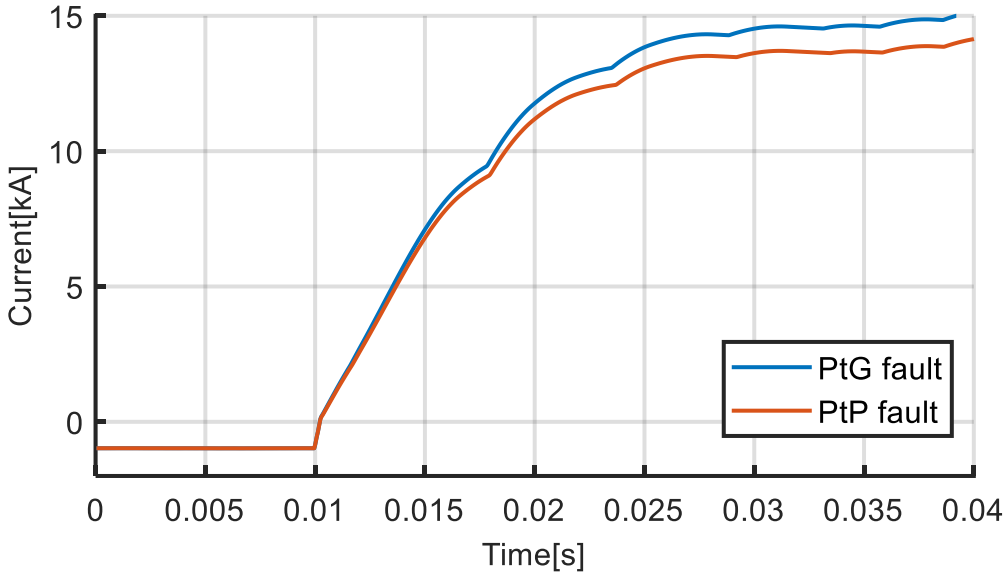

Figure 180 Comparison of fault current evolution; PtG fault (blue), PtP fault (red)

As discussed in section 7.5.3 the current breaking capability can be determined by the STB for primary protection with two ideal voltage sources for the representation of adjacent feeders (see Figure 121). This is the result of the sensitivity analysis. In fact, all CBC requirements for primary protection are higher compared to the backup protection case. Figure 181 shows additional results for a slow breaker failure identification time of 3ms (T_{BFI}=1ms).

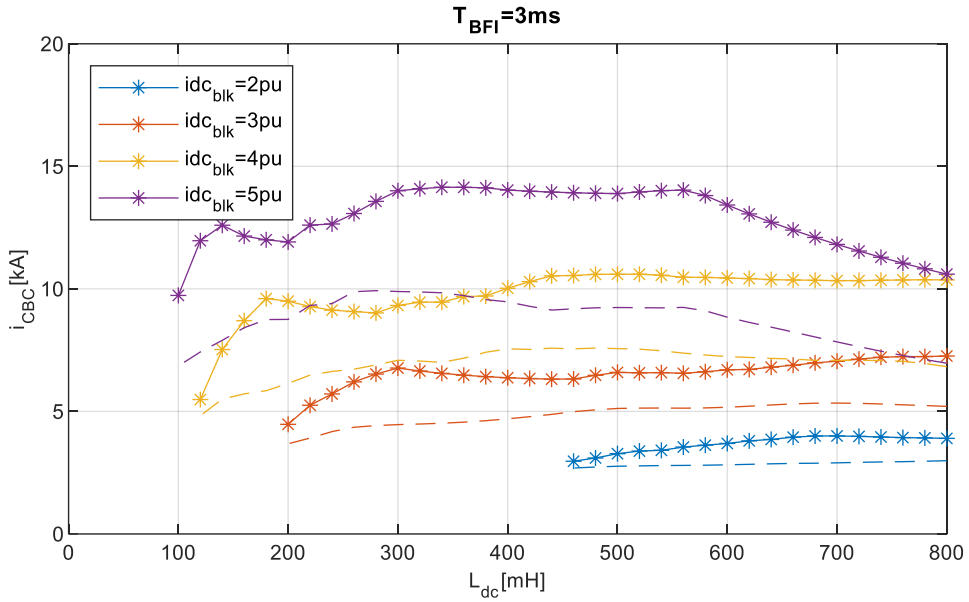

Figure 181 Comparison between CBC requirements for primary protection (solid) and backup protection (dashed); T_{BFI}=3ms

12.4. Use case 1.1 validation for protection studies

In this section use case 1.1 simulation results from detailed and simplistic models are compared.

→ Detailed: Averaged arm MMC models, wideband cable models, detailed DCCB models with IGBTs and surge arrester

→ Simplistic: Averaged value DC MMC models (see section 5.3), pi-section cable models (see section 5.1), simplistic DCCB model (see section 5.5)

Figure 182 shows the simulation results for a primary protection sequence with spoke fault on L2 (0km from Bb2). Use case simulation with detailed models and simplistic models are respectively depicted in blue and red color. The fault occurs at T=0ms. At T=6.5ms the DCCB holds the TIV of 1.6pu which leads to a decrease of fault current. At T=17ms the magnetic energy is absorbed, and the fault current is suppressed. The converter remains operational as the DC current blocking limit in this simulation case is set to $i_{dc,blk}$=9.525kA (5pu). Comparing simplistic and detailed simulation results it can be concluded that the curves are of similar shape during the entire fault current interruption process. Especially the peak current for both spoke and MMC as well as the fault current suppression time are well represented by the simplistic simulation case. The converter current oscillation after fault current suppression shows the same frequency but is more damped for the detailed use case simulation. The energy absorption of the DCCB is overestimated by the simplistic model.

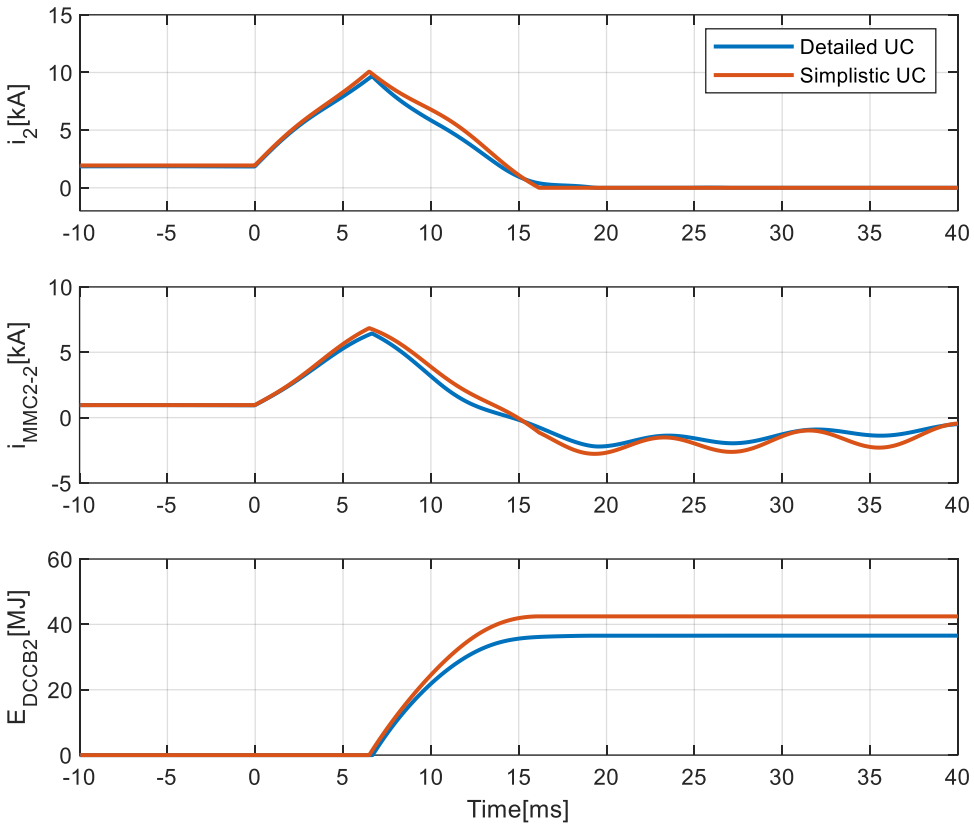

Figure 182 Results for primary protection sequence (spoke fault on L2), comparison between Use case simulation with detailed models (blue) and simplistic models (red); Top=6ms, Ldc=220mH, idc,blk=5pu

In Table 86 use case simulation results obtained by detailed models are compared to use case simulations with simplistic models.

Table 86 Results of maximum MMC currents and maximum spoke currents for Use case 1.1 primary protection simulations during spoke fault at offshore side of L2; Comparison between use case simulations with detailed models and simplistic models

MMC 2-2 current

idcblk[pu]	**3**	**4**	**5**
Top[ms]	**[%]**	**[%]**	**[%]**
2	1,33	0,24	-1,01
4	-2,09	-3,93	-5,19
6	-3,31	-5,09	-6,38
8	-4,73	-6,18	-7,65
10	-4,77	-6,44	-8,08

Spoke L2 current

idcblk[pu]	**3**	**4**	**5**
Top[ms]	**[kA]**	**[pu]**	**[kA]**
2	0,67	0,38	-0,23
4	-1,57	-2,50	-3,17
6	-2,47	-3,33	-4,04
8	-3,59	-4,29	-5,05
10	-3,80	-4,41	-5,17

It can be concluded that use case simulations with simplistic models provide a good approximation of fault current estimations. To increase the sensitivity analysis variation simplistic models are used for use cases 1.2 and 2 simulations as shown in section 7.8.